

VLSI Implementation of a High Speed and Area Efficient N-bit Digital CMOS Comparator

M.MADHAVI
Assistant Professor
Department of ECE
DRK INSTITUTE OF SCIENCE AND
TECHNOLOGY
Hyderabad, India
madhavi.marripally@gmail.com

B. Haripriya,
Assistant Professor
Department of ECE
DRK INSTITUTE OF SCIENCE AND
TECHNOLOGY
Hyderabad, India
boinapally.haripriya416@gmail.com

ABSTRACT: Comparing two numbers that are greater than, less than, or equal to one another is one of the most basic arithmetic comparisons in a digital comparator. A digital comparator requires additional room to do large-scale arithmetic comparisons, which increases power consumption and causes a delayed response. An N-bit comparator with two modules and 45 GPDKCMOS technology can be used to solve this. The space and power consumption of the suggested comparator design can be decreased by using an N-bit comparator, which can function at incredibly high speeds with effective area and power dissipation. Starting with the least significant bit and going all the way up to the most significant bit, the suggested model is implemented bitwise. A parallel prefix tree structure is the end product of this procedure, which only proceeds if the bits are equivalent. The suggested comparator structure approach consists of two separate

modules: the comparison evaluation unit (CEU) is the second unit, and the final unit (FU) is the first. Tree topologies are made using verified results from the systematic arrangement of repeated logic units. The FU module authenticates the result by relying on CEU results. The proposed architecture's use of structured VLSI technique enables area derivation using analytical method relating transistor count and total delay, which can be understood in terms of operand bit width. While running the virtuoso simulations at 1 GHz with both old model and 45 GPDK CMOS technology, it has been found that the design has been enhanced the operating speed by 31.92% while reducing power usage by 77.76%.

KEYWORDS: GPDK, CMOS, CEU, VLSI, COMPARATOR.

I.INTRODUCTION: A digital comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater

than, less than or equal to other number. It can be used in several applications such as IR sensors, OP-amp's, Image processing etc. In one of the previous designs [1-9], an eight transistor XOR-XNOR(XE) with cross-coupled P-MOS, is used to design the comparator and it helps in improving the speed and power efficiency. But it is not applicable in the increased bit-widths because if the bit width increases it can't be able to produce full swing output voltage. In another design [8], it uses different logic techniques for the comparison of transistor count, power consumption and propagation delay. And to improve the propagation delay a hierarchical prefix tree structure method had been proposed [10]. However, the power consumption will be more for $\log_2 N$ comparison levels for the wide input operands. Several comparator designs have also been verified like parallel prefix tree structure's, dynamic logics, using subtractors or multipliers in the designing process etc. each having several specifications. In the evolving VLSI technology, it is important to design any electronic component with less area and improved power efficiency and operating speed. In this paper we are designing the comparator which is efficient in terms of speed, power consumption and area. To

improve the power consumption, we have used parallel prefix tree structure method, and to produce the full swing output voltage a novel EX-OR-NOR cell had been considered from [3].

II.MOTIVE: CMOS N-bit digital Comparators are essential for this project. Two binary numbers used, and compared based on their magnitude. There is a possibility that one of the two numbers will be bigger, less, or equal to the other. A digital circuit known as a digital comparator performs the operation of comparing two binary numbers. The digital comparator is the backbone of many different types of designs. Output is derived from a process that includes comparison. This output is used to determine the final findings.

III.EXISTING SYSTEM: First, A transmission gate using NMOS and PMOS transistors created connected in parallel. The transmission gate is fundamentally an AND gate. A resistor is attached to the output terminal of the Transmission gate since its output is unreliable. At the complementary NMOS and PMOS gate terminals, control signal A is applied. If the Logic 1 is input, and the command signal is logic. Input logic 1 turns on PMOS and turns off NMOS, while logic 0 turns off PMOS and turns on CMOS. If the output will be logic 0 if the

control signal is logic 0 inverse of what was input. In the following circuit schematic, the NMOS transistor is ON and the PMOS transistor The NMOS transistor is disabled and the output current can flow through it when the control signal is a logic1. The output current is conducted by the PMOS transistors when the control signal is logic 0, turning off the NMOS. Logic 0 at the input turns off PMOS and turns on CMOS activated. The logic of the control signal state of '0' indicates that the output is equal to the control, and vice versa.

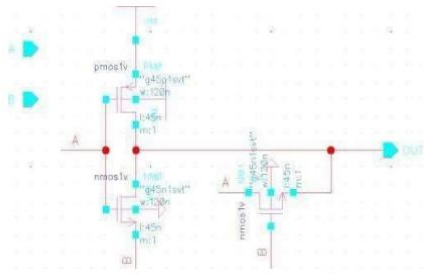


Figure 1: XOR Gate using TG

IV. PROPOSED SYSTEM: In order to lower the space no of gates can be reduced. The above circuit can be made simpler by the logic of AB and $A=B$, as shown in figure. As you can see from the diagram above, in addition to the inverters, the 4-Bit comparator using 11 gates can also be created. Gates of this type include XOR, AND, and NOR. The four XOR gates are identical. Although the number of inputs for the five AND gates vary, the basic concept remains the same. The NOR gate also does.

The circuit shown above uses a variety of AND gates. The circuit consists consisting of four XOR gates, five AND gates accepting inputs ranging from two to five, four inputs, and two outputs. NOR inputs and 5 inverters, as can be seen from the simplified logic diagram. Time and space were chosen by the measures of performance to be used in the design process. Taking into account the use of performance metrics such as t_d , t_{phl} , t_{plh} , area, power dissipation, and others metrics demonstrates that area is advantageous for pseudo Nmos. Propagation delay, T_r , and T_f are all aspects of temporal performance that can take into consideration in this paper.

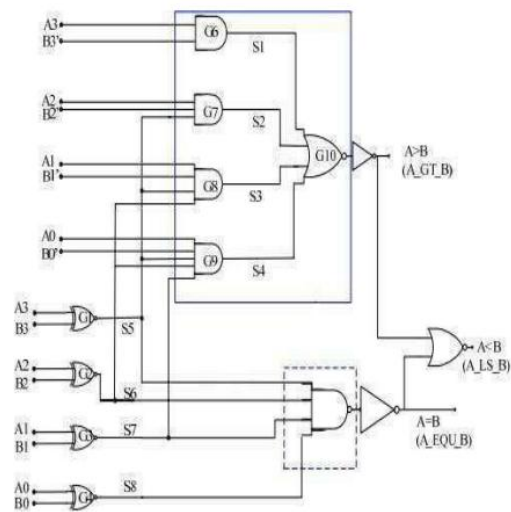


Figure 2 Diagram of the proposed scheme
And others metrics demonstrates that area is advantageous for pseudo-Nmos. Propagation delay, T_r , and T_f are all aspects of temporal performance that can take into consideration

in this project. Propagation was chosen as the first index because, This the SS1 block is far more complex than the remainder of the circuit, as seen by the simplified logic diagram components. The size start with is $W_{p_eff}=1.73W_{n_eff}$. To make T_r equal to T_f in previous blocks, $W_{p_eff}= 3W_{n_eff}$ was used. From the design it was observed that the circuit utilizes a 4 input NOR. Generally, it is known how expensive NOR gates are.

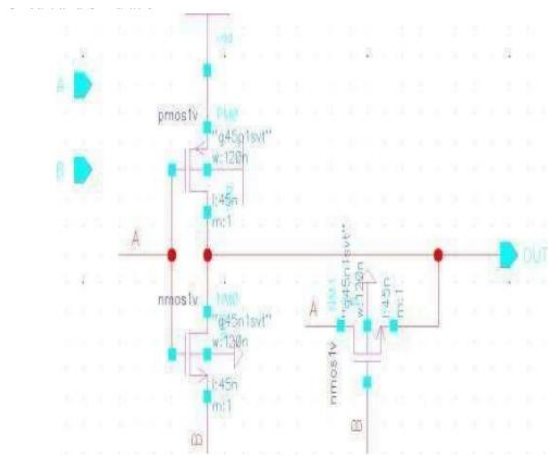


Figure 3 Diagram of the proposed scheme This places more strain on the driver circuit in terms of space, Power, delay, output load capacitance (as a result of input capacitance and drain diffusion capacitance both increase as drain temperature rises. are all affected... for the same performance. Normally, switch to NAND and avoid using a big fan in NOR. However, since the fan-in for this project is only 2, 2 inputs NOR gates are used for practice, and test the

performance to obtain precise information with which to compare the characteristics. Here, the XNOR, NOR, SS1, and SS2 components of the comparator design were shown and measure it after simulation.

V.RESULTS: The complete comparison process consists of Sets 1-4 are in CEM, and Set 5 is in FM. According to their utility, all of the design's sets are arranged in a hierarchical four-prefix arrangement and the output in this manner, each set acts as the input. to the next; the only exception is set 1, whose outputs are fed into both sets 2 and 3. In set 1, the novel The EX-OR-NOR cell compares two binary operands of N bits each. Bit-by- bit. Using CMOS and pass transistor logic, a design for an EX-OR-NOR cell is proposed. It performs EX-OR and EX- NOR functions with only seven transistors instead of the usual eight. Transistor M5 is utilized to make EX-NOR's full output voltage swing possible. Although the six-transistor architecture as described in, when the input operands are small, the output voltage swing is modest set to zero or one.

The proposed EX-OR-NOR cell consists of seven transistors (M1M7), four of which are P- channel metal oxide semiconductors (PMOS) and three of which are N channel MOS (NMOS). PMOS transistor in the

feedback while boosting the output with CMOS logic to accommodate a wide range of voltages at the EX-OR gate's output terminal transistor logic and CMOS logic. It uses seven transistors for EX-OR and EX-NOR operations as compared with the conventional eight transistors model. The M5 transistor is utilised to obtain full output voltage swing of EX-NOR operation as shown. The six transistors model has also been reported in but it gives limited output voltage swing when applied input operands are (0, 0) or (1, 1). Optimum aspect ratios of the seven transistors (M1–M7) consisting of four P channel MOS (PMOS) and three N channel MOS transistors of the proposed EX-OR-NOR cell are carried out to avoid the universal drive constraint faced by the pass transistor logic.

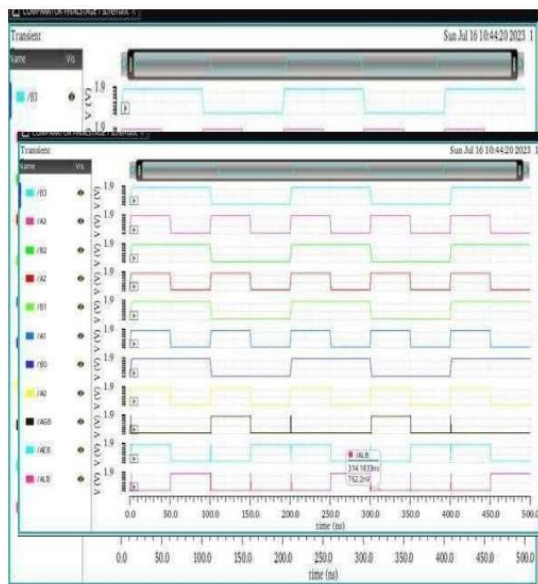


Figure 4 Proposed schematic of 4 Bit Comparator simulation

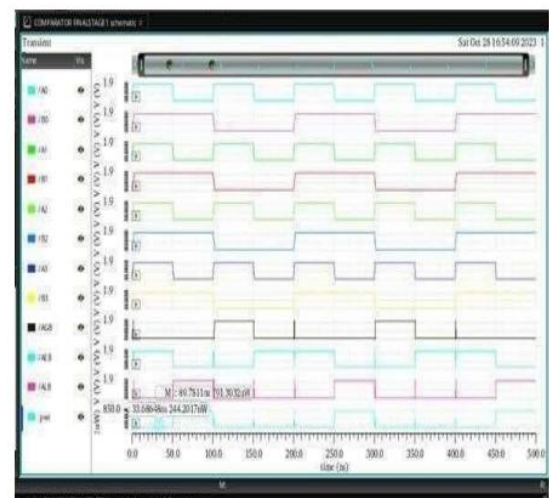


Figure 5 Dynamic power Simulation

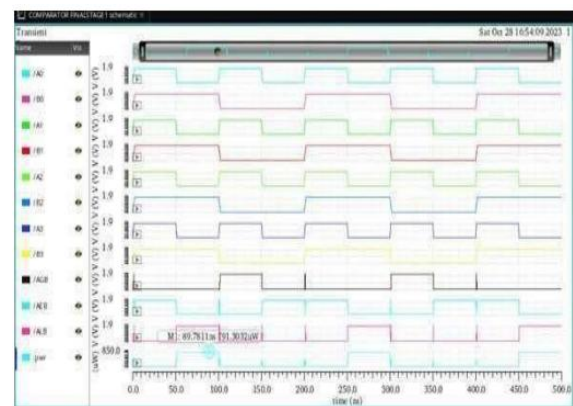


Figure 6 Static power simulation

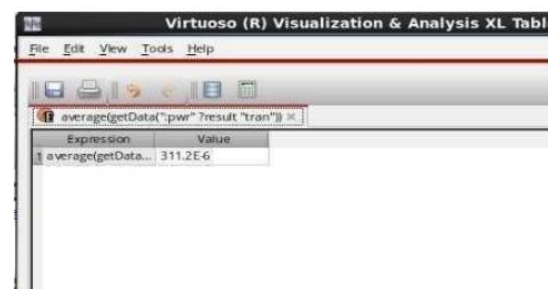


Figure 7 Average power

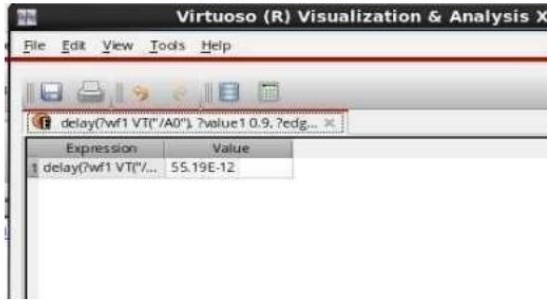


Figure 8 Delay simulation

When employing a traditional method, the final integrated circuit's performance is optimized when the complex interplay of chemical, thermal, and photographic factors is thoroughly understood and controlled. behaviour is heavily reliant on the placements and connections of the geometric shapes. The layout engineer, often called a layout technician, is responsible for the physical arrangement and wiring of all the parts. of the chip using a computer-aided designing tool such that it satisfies a set of requirements, most frequently performance, size, density, and manufacturability. The two main layout disciplines of analog and digital are frequently separated out into separate practices.

Table 1 Table of analysis

S.NO	Method	Power (nW)	Delay (nsec)	No. of Transistors (area)
1	Existing Method [8]	121.97	140.73	175
1	Existing Method [6]	58.97	70.73	113
2	Proposed Method	01.53	50.02	80

VI.CONCLUSION: In this study, a scalable comparator using comparative

evaluation and modules is chosen. Reiterated logic cells, a typical structure in the CEM, are used to create the parallel prefix tree structure. The typical predictions of the suggested comparator are assessed using regular structure for any arbitrary bit widths. It was discovered that using 45 GPDK CMOS produced the maximum working frequency with the least amount of power dissipation and delay. The opted comparator is favoured for many applications, such as memory addressing logic and scientific computations, due to these advantages. A scalable comparator is suggested using the comparison evaluation module and final module. Reiterated logic cells, a frequent structure in the CEM, are used to implement the parallel prefix tree structure. For arbitrary bit widths the characteristic predictions of proposed comparator is done using this regular structure. While as compared with the prevailing comparators which can be designed the usage of 0.18 μm CMOS era the working frequency is maximum, F04 delay is minimal and power dissipation is very low for the proposed comparator. These merits of the comparator which is proposed makes it fit for several packages such as memory addressing logic, scientific computations.

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