

**POWER FACTOR CORRECTION METHODS DESIGN AND ANALYSIS
FOR SINGLE PHASE CONVENTIONAL AND INTERLEAVED DOUBLE
BOOST CONVERTERS**

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Abstract:

One of the most crucial circuits in small and medium-sized power supplies where the intended power flow is unidirectional is the diode rectifier. The AC input power is frequently distorted by the capacitor connected in parallel to the load of such power supplies, resulting in extremely high THD and poor power quality, which lowers the input power factor. The input current is reshaped to be sinusoidal and the power factor is raised to a value as high as one by using power converter interfaces and manipulating the duty cycle so that the entire power converter and load are perceived as totally resistive. Therefore, a thorough analysis of these power factor correction circuits (PFC) with two power converters is provided in this paper: Interleaved Double-Boost Converter (IDBC) and Conventional

Boost Converter (CBC). The investigation continues with the creation of a control loop and a steady state model. Two loops are used in the control scheme: a slower outer voltage loop and a quicker inner current loop. Bode plots and other frequency response approaches are used throughout the control loop design process, with a focus on establishing appropriate bandwidth and phase margins to guaranty that the controller speed and overshoots are within acceptable bounds. Lastly, the CBC and IDBC results are shown with a focus on guaranteeing higher THD and power factor levels.

Keywords: Power factor correction, boost converter, interleaved double boost converter, and controller design are index terms.

1.Introduction:

In many electrical and electronic applications, DC power supply are utilized. While capacitors lessen DC ripple, diode rectifiers transform AC to DC. Capacitive filters, however, pull non-sinusoidal current, which results in low power factor and excessive THD[1]. Thus, PFC methods are employed to enhance power quality and input-current waveform.

1.1 Feedback Control and Active Power Factor Correction:

The input current is shaped by an active PFC to match the input voltage. In order to minimize harmonics and attain a power factor near unity, a boost converter with feedback control modifies the switch duty cycle. Under various circumstances, the controller also controls the DC output voltage[2].

1.2 Active PFC's Limitations with Output Voltage Control:

An active PFC system's voltage loop is typically slow, which can result in output-voltage ripple and a sluggish reaction to changes in load. For quicker voltage regulation and less output ripple, an extra DC-DC converter might be utilized.

1.3 Designing Feedback Loops for Adaptive Control and Stability:

Under changes in input and load, the feedback loop keeps the PFC operating

steadily. High power factor, reduced THD, strong voltage regulation, and consistent performance are all provided by a well-designed controller[3]. PFC performance can be further enhanced by sophisticated methods like feed forward and adaptive control.

2. Existing System

For power factor adjustment, the current system employs a conventional boost converter (CBC) after a single-phase diode bridge rectifier. A sizable DC-link capacitor is typically linked across the load in traditional AC-DC power systems[4]. The input current becomes extremely distorted and discontinuous as a result of the capacitor charging close to the input voltage peaks. This leads to a decrease in power factor and an increase in input current THD. A traditional boost converter is used as a PFC stage to solve this issue. A quick inner current-control loop and a slower outer voltage-control loop make up the converter's two-loop control structure. In order to improve the power factor and lower current harmonics, the duty ratio is adjusted so that the input current follows the sinusoidal input voltage waveform.

2.1.Disadvantages :

1. High Input Current THD

2. High Current Stress on Components
3. Higher Switching Losses
4. Large Inductor Requirement
5. Higher Current Ripple
6. Limited Power Handling Capability
7. Thermal Management Issues

3. Proposed System:

Instead of using a traditional single boost converter as the PFC stage, the suggested solution uses an Interleaved Double Boost Converter (IDBC). The interleaved converter is made up of two boost converter phases that share the input current by working with a phase shift, typically 180° . The two interleaved boost stages receive the rectified voltage after the AC input has first been converted via a diode bridge rectifier. A quick inner current loop and a slow outside DC-voltage loop make up the two-loop control method used[5]. While the outer loop controls the DC output voltage, the inner loop molds the input current to resemble the reference sinusoidal waveform. Interleaving spreads current between the two switching devices, lowers semiconductor stress, enhances thermal performance, and lessens input and output current ripple. Therefore, as compared to the traditional boost PFC design, the suggested system can

accomplish better power-factor correction and lower THD.

3.1. Advantages:

1. Reduced Input Current THD
2. Improved Power Factor
3. Reduced Current Ripple
4. Reduced Semiconductor Stress
5. Improved Thermal Performance
6. Higher Power Capability
7. Better Dynamic Performance

4. Problem Statement:

Highly distorted and non-sinusoidal currents are drawn from the AC supply by conventional single-phase AC-DC power supplies that use capacitive filters and diode bridge rectifiers. Low power factor, high input current THD, increased harmonic pollution, and inefficient use of the electrical supply are the outcomes of this[6]. Because the entire input current travels through a single power-processing path, a traditional boost converter faces significant current stress, relatively high current ripple, and increased thermal stress even though it can be utilized as a PFC stage to optimize the input current waveform. Consequently, an enhanced PFC topology that may lower input current distortion, increase power factor, lower current ripple, and distribute electrical and thermal stressors among several switching

devices is required. By creating and evaluating an Interleaved Double Boost Converter (IDBC) with appropriate inner current and outer voltage control loops and contrasting its performance with a traditional boost PFC converter under comparable operating conditions, the proposed work tackles this issue[7].

5.Objective :

The main objective of this project is to design and analyze conventional and interleaved boost converters for active power factor correction[8]. The system aims to achieve high power factor, low input current THD, reduced current ripple, stable output voltage, and improved converter efficiency using suitable feedback control techniques.

6. Literature review:

6.1. Han (2024), Han studied a continuous-conduction-mode boost PFC converter for improving input power quality. The study focused on reducing input-current harmonic distortion under different load conditions. A frequency-modulation technique was investigated to improve PFC performance, especially at light loads. The converter was analyzed in terms of input current, THD, and power factor. The results showed improved current waveform quality and reduced harmonic distortion. This

work provides a useful basis for conventional boost PFC design.

6.2. Li et al. (2024), Li et al. investigated a data-driven compensation method for an interleaved boost PFC converter[9]. The method was developed to improve grid-side power quality and current tracking. The study considered nonlinear characteristics and control delays in the converter. Interleaving was used to distribute current between multiple converter phases. The proposed approach improved the input-current waveform and PFC performance. This work is relevant to the analysis of interleaved boost converter control.

6.3. Yoon et al. (2024), Yoon et al. studied current balancing in an interleaved boost PFC converter. An auxiliary-winding coupled-inductor technique was used to improve current sharing. The approach reduced the current imbalance between the two interleaved converter phases. The converter performance was investigated through simulation and experimental testing. The results demonstrated improved current balancing and reliable converter operation. This work supports the use of interleaving for reducing component current stress.

7. Implementation methodology:**7.1. Passive Power Factor Correction**

Using passive parts like inductors, capacitors, and LC filters, Passive Power Factor Correction (PFC) lowers harmonic distortion and raises power factor. When compared to active PFC technologies, it is straightforward, dependable, and economical[10]. Distribution networks, HVAC systems, lighting systems, and industrial motors all frequently use passive PFC. Capacitors can increase electrical efficiency and make up for reactive power. Passive PFC, on the other hand, is less effective under changing load conditions and offers set compensation. Large capacitors and inductors can add bulk to the system and raise its cost. Resonance danger, component aging, maintenance needs, and a lack of dynamic control are some of its drawbacks.

7.2. Active Power Factor Correction:

Active Power Factor Correction (PFC) dynamically shapes the input current based on the input voltage using power electronic switches, controllers, and feedback circuits. Compared to passive PFC, it offers superior power-factor correction and reduced harmonic distortion. MOSFETs and other switching devices are managed by varying the converter's duty cycle.

Active PFC can retain superior performance throughout a range of load scenarios and reach a power factor that is almost equal to unity. It is frequently utilized in high-efficiency electronic devices and contemporary power supply[11]. Current-source and voltage-source active PFC converters can be generically categorized. In real-world applications, voltage-source PFC converters are more frequently utilized.

7.3. Active PFC Topologies: Current-source and voltage-source converters are the two primary categories of active PFC topologies. While voltage-source PFC converters can be based on buck, boost, buck-boost, and Cuk converter architectures, current-source PFC converters typically use buck-type designs[12]. Because of their efficient input-current shaping and voltage conversion properties, boost and buck-boost converters are among the most popular. The necessary output voltage, power level, efficiency, and control needs all influence the topology choice.

7.4. Boost Topology

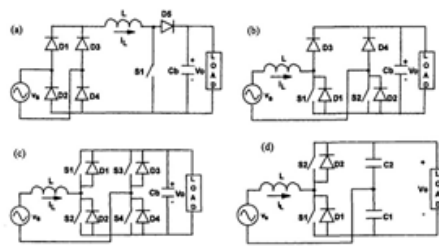


Fig.1: Different. Topologies in Boost PFC Topology. (a) Single Switch (b) Two Switch (c) Four switch (d) Half Bridge

7.4.1. Boost Converter for Active PFC:

The **boost converter** is widely used in active PFC because it provides a continuous input current and a DC voltage gain greater than unity[13]. The conventional single-switch boost converter is simple, easy to control, and can operate in **CCM, BCM, or DCM** modes. Its large input inductor reduces switching-current ripple and minimizes input-filter requirements. Due to its simple structure and good performance, it is commonly used in **medium- and high-power PFC applications**.

7.4.2. Buck-Boost or Fly back Topology

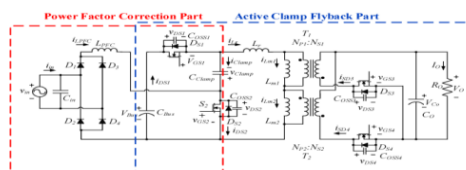


Fig.2: Flyback based PFC with active clamping Technique.

7.4.3. Flyback PFC Converter: The flyback PFC converter offers straightforward control and easy galvanic isolation between input and output, making it primarily appropriate for low-power applications[14]. In contrast to the boost converter, it includes basic overload protection and can produce an output voltage that is either higher or lower than the peak input voltage. Flyback PFC converters can function in either CCM or DCM, with DCM being more widely used because to its straightforward control and removal of diode reverse-recovery issues. Nevertheless, in comparison to boost PFC converters, the discontinuous input current generates more noise and EMI.

7.4.4. Buck Topology

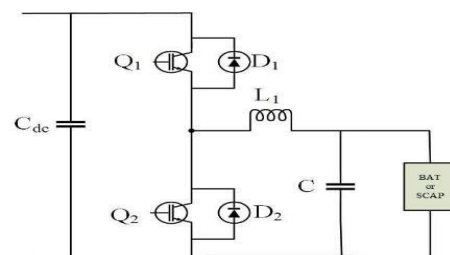


Fig.3. Circuit of Half Bridge Based Buck Converter

7.4.5. Buck PFC Converter:

When the necessary output voltage is less than the input voltage, the buck PFC converter is appropriate. The converter is unable to draw current when the input voltage drops below the output voltage, which causes the input

current to become distorted[15]. By operating in buck mode at higher input voltages and boost mode at lower voltages, a buck-boost arrangement can get around this restriction and preserve a sinusoidal input current. Current-source buck PFC converters have good current-limiting capabilities and can draw sinusoidal current over the whole input-voltage range. They are especially helpful for applications like DC motor drives and AC-DC rectifiers that need low output voltage and over current prevention.

8. Design of Conventional and IDBC PFC:

In this section, design and analysis of active power factor correction for conventional and IDBC converters are presented in detail. The control loops are designed and discussed.

8.1 Design of Active CBC based Active PFC:

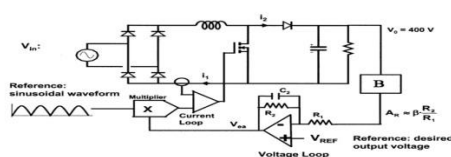


Fig.4. Schematic of CBC based PFC with control loop.

8.2. Conventional Boost-Based PFC Converter:

A standard rectifier's capacitive filter is swapped out for a boost converter in a conventional boost PFC converter. A diode bridge is first used to convert the AC input to DC. The boost converter, where the inductor, switch, diode, and capacitor regulate the energy flow and raise the voltage, receives the rectified voltage after that[16]. By controlling the switch with PWM, the input current is shaped to follow the input voltage, increasing power factor and lowering harmonics. The output capacitor lessens ripple and smooths the DC voltage. To maintain the necessary output voltage, a feedback controller monitors the output voltage and modifies the PWM duty cycle.

8.3.Steady-State Analysis and Control Scheme of Boost PFC:

The Boost PFC converter helps to achieve a high-power factor close to 1, indicating efficient use of electrical power. This is important for reducing power losses, minimising harmonics, and complying with regulations such as those outlined in the IEC 61000-3-2 standard for power quality. The parameters necessary are listed in Table.1

Parameter	V _m (Peak)	Line- frequency	Switching frequency (f _{sw})	Output Voltage (V _o)	Current Ripple (%)	Voltage Ripple (%)	Load Current (I _o)
Value	325 V	50 Hz	100 kHz	400 V	10	1	5 A

Table 1: Parameters for Steady State Design

$$D = 1 - \frac{V_m}{V_o} = 0.1875.$$

$$L = \frac{V_m D}{f_{sw} \Delta I_L} = 990.2 \mu H$$

$$C = \frac{D}{\Delta V_o f_{sw}} = 2.343 \mu F$$

Equations are used to obtain the values of L and C using the parameters in Table 1. With the exception of the voltage loop's extremely narrow bandwidth—much less than 100 Hz—and the fact that the current reference produced by the outer loop is not constant but rather has the shape of $|\sin(\omega t)|$, the control method of a PFC is remarkably similar to that of average current control. Therefore, the methods covered in average current control served as the foundation for the control scheme that is provided here[17]. The PFC's streamlined loop construction

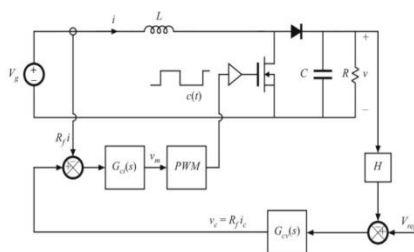


Fig.5. Simplified closed loop representation for demonstrating average current control in PFC.

8.4.Small-Signal Modeling and Control Design of CBC Converter:

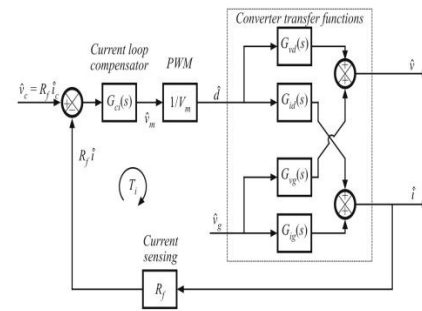


Fig.6. Block Diagram Representation of the small signal model of CBC converter

$$T_i = R_f G_{ci} \frac{1}{V_m} G_{id}$$

Here, R_f is the gain of the current sensor, G_{ci} is the compensator (PI) of the current controller, V_m is the PWM gain and G_{id} is the transfer function relating current to duty ratio. G_{id} is given by,

$$G_{id}(s) = \frac{2V_o}{R(1-D)^2} \frac{1 + \frac{s}{\omega_{zi}}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

$$\text{Where, } \omega_{zi} = \frac{2}{RC} \text{ and } Q = R \sqrt{\frac{C}{L}}$$

Using Equation 3.4 and 3.5, G_{ci} is designed such that T_i has a bandwidth of $\frac{f_{sw}}{10}$ and the Phase margin is >60 degree. With this inner loop closed[18], control to voltage transfer function $G_{vc}(s)$ is given by Equation.

$$G_{vc}(s) = \frac{1}{R_f} \frac{G_{vd} T_i}{G_{id} (1 + T_i)}$$

To design the compensator, the voltage loop gain is derived and is given by equation

$$T_v = H G_{cv} G_{vc}$$

In this case, H is the voltage sensor's feedback gain and G_{cv} is the voltage loop compensator. The voltage loop

TV is made so that the PM is at least 45 degrees and the outer voltage loop's bandwidth is less than 100 Hz.

To design the controller for PFC, following are the parameters chosen as in Table.2

Parameter	VM	H	R_f	Bandwidth of inner loop	Bandwidth of inner loop
Value	4	3/400	0.25	10kHz	10 Hz

Table.2 Parameters to design controller for CBC converter

8.5. Design of Active IDBC based Active PFC:

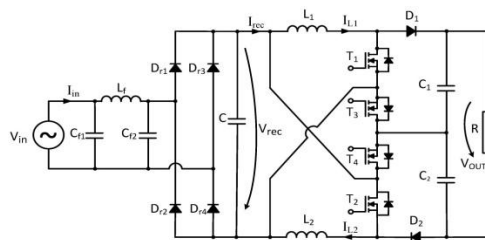


Fig.7. Proposed schematic of the IDBC converter

The Independent Double Boost Interleaved Converter (IDBIC), a special DC-DC power-stage topology, is the foundation of the suggested PFC application. The fundamental PFC converter topology serves as the foundation for the existing architecture. The values of the passive components utilized in the converter are determined using standard steady state averaging techniques and are shown in Table 3.

Parameter	L_1	L_2	C	C_1	C_2	R
Value	0.5mH	0.5mH	10mF	500nF	500nF	100 Ohms

Table.3 Design Values of IDBC Converter

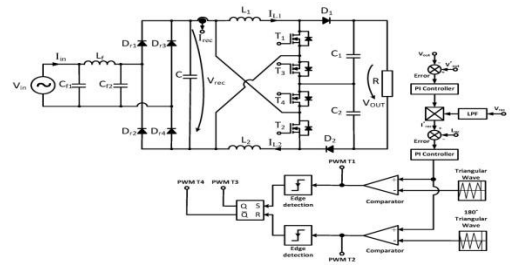


Fig.8. Schematic of the IDBC converter along with control scheme used for PFC application.

With a slow-acting outer voltage loop with a bandwidth of about 10 Hz and a fast-acting inner loop with a bandwidth of about 1/10th of the switching frequency, the control is very similar to the CBC converter. The peak current is determined by the voltage loop compensator's output, and the voltage across the diode rectifier terminals synchronizes the current loop's structure. Based on the discrepancy between the reference current and the actual current, the SR flip-flop modifies the converter.

9. PID Controller :

One popular feedback control method in industrial systems is the PID (Proportional-Integral-Derivative) [19] controller. It determines the difference between the measured process value and the intended set point and modifies the control input to minimize this difference. Three terms make up the controller: derivative (D), integral (I), and proportional (P). The D term

forecasts future error based on the rate of change, the I term takes into account cumulative past errors, and the P term reacts to the current error. The PID controller can ensure steady operation, lessen overshoot, and enhance system response by adjusting these settings. Depending on the application, one or more terms may be omitted, resulting in P, PI, or PD controllers. PI control is widely used because derivative action can be sensitive to measurement noise.

1) Interactive Algorithm

$$\bar{n}(t) = K_C \left[e(t) + \frac{1}{T_i} \int_0^t e(\tau) d\tau \right] * \left[1 + T_d \frac{d}{dt} e(t) \right]$$

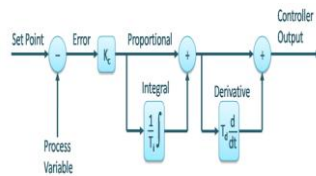


Fig.9. Interactive Algorithm

2) Non Interactive Algorithm

$$\underline{u}(t) = K_C \left[e(t) + \frac{1}{T_i} \int_0^t e(\tau) d\tau + T_d \frac{d}{dt} e(t) \right]$$

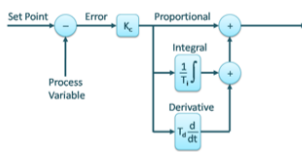


Fig. 10. Non Interactive Algorithm

9.1. Proportional Term: The proportional term produces an output proportional to the present error. It is controlled by the proportional gain (Kp). A higher (Kp) gives a faster

response but may cause overshoot or instability, while a lower (Kp) gives a slower response. Proper tuning of (Kp) provides suitable control action and system stability.

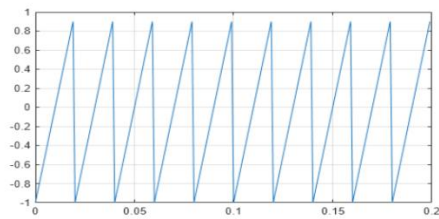
9.2. Integral Term: The integral term depends on the accumulated error over time and is controlled by the integral gain (Ki). It helps eliminate steady-state error and moves the system toward the desired set point. However, excessive integral action can cause overshoot and slower system response.

$$i_{out} = K_i \int_0^t e(\tau) d\tau$$

9.3. Derivative Term: The derivative term responds to the rate of change of the error and is controlled by the derivative gain (Kd). It predicts the future trend of the error and helps reduce overshoot and improve system stability. However, derivative action can be sensitive to measurement noise.

9.4. Sawtooth Wave: A sawtooth wave is a non-sinusoidal waveform that increases or decreases gradually and then changes sharply in the opposite direction. It is commonly used as a reference or carrier waveform in power-electronic switching and control applications.

$$D_{out} = K_d \frac{d}{dt} e(t)$$



For the elements of the time array t , $x = \text{sawtooth}(t)$ produces a sawtooth wave with period 2π . Sawtooth is comparable to the sine function, except it produces a sawtooth wave with maxima of -1 and 1 . The sawtooth wave is defined as increasing linearly with a slope of $1/\pi$ at all other times and becoming -1 at multiples of 2π .

10. Results and Discussion:

10.1.CBC Based Active PFC:

In this section, the results of CBC based active PFC is presented in detail. This section starts with results from controller design followed by the results from PFC converter.

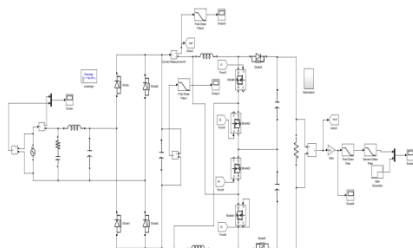


Fig.11. Simulation model

The PFC starter response is depicted in Fig., where the DC output voltage increases from 0 V to the 360 V reference. It takes about 0.15 seconds

to settle. Good power factor is indicated by the sinusoidal and in-phase grid voltage and current[20]. The grid-current THD of 3.10% in the figure satisfies the necessary IEEE power-quality limits.

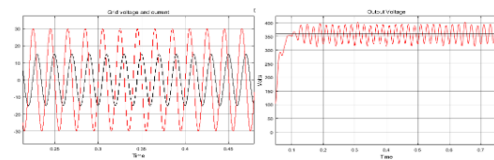


Fig. 12 Grid Voltage and Current along with output voltage waveforms for CBC

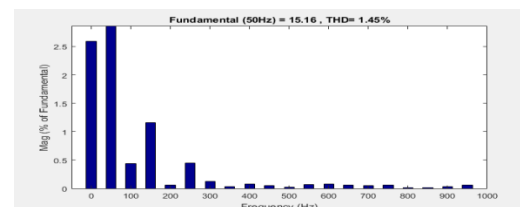


Fig. 13 FFT spectrum of AC Line Current for Resistance $R=80\text{ Ohms}$ and $V_{ref} = 360\text{ V}$

Additionally, a 16.66% increase in load is applied to the PFC converter; the results are shown in Fig. 5.4. In 0.2 seconds, the controller returns the voltage to the reference value of 360 V . Higher peaks in grid current indicate that as the load increases, so does the power drawn from the source. Once more, the power factor is kept at 1 .

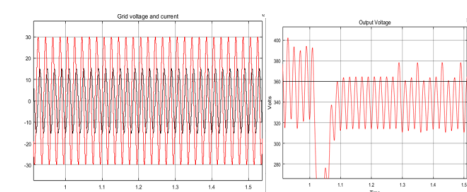


Fig.14 Response of PFC for step change in Load from R to 83% of R

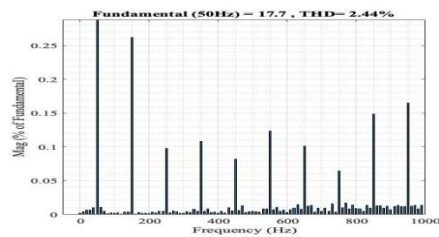


Fig.15 FFT spectrum of AC Line Current for Resistance $R=66.66$ Ohms and $V_{ref} = 360$ V

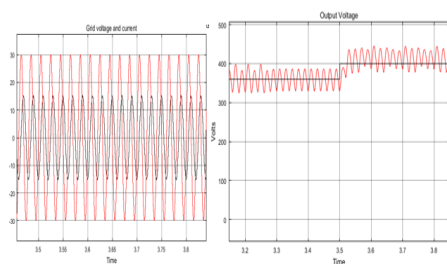


Fig.16 Response of PFC for step change in reference from 360 V to 400 V

Fig.16 Response of PFC for step change in reference from 360 V to 400 V

Above Fig. shows the results of changing the reference command to the PFC from 360 to 400V in order to verify the controller's robustness. The reference can be tracked by the controller in 0.2 seconds. Higher peaks in grid current indicate that as the load increases, so does the power drawn from the source. Once more, the power factor is kept at 1.

11. Conclusion:

This paper provides a detailed discussion of diode rectifier-based unidirectional power sources, which are used in everything from satellite/propulsion systems to laboratory equipment. The non-linear

AC current extracted from utilities by the charging and discharging of filter capacitors attached to the diode rectifier's output terminals is one of the main issues with such rectifier systems. According to the study and findings in the thesis, these effects are sometimes so harmful that the THD drawn is more than 170% and the power factor is less than 0.5. There is also discussion of potential solutions to these issues, which fall into two categories: passive PFCs and active PFCs. Connecting an LC filter to the diode rectifier's terminals is one passive option.

These line reactors may not be a practical choice due to their large diameters and the filters' 100 Hz construction. Additionally, two converters—CBC and IDBC—are used in the design of active solutions. The goal of active solution is to precisely match the input current to the converter with the voltage across the rectifier's terminals by shaping the duty cycle. The results are provided in detail, and a control method is devised for the same. The suggested control approaches can match the grid voltage and current so that the power factor is unity and the current has a sinusoidal shape. Additionally, the THD for the same is shown.

12. Future Scope:

According to the boost/IDBC converter paper, the future scope of PFC covers the following important points:

- 1) GaN/SiC semiconductors are being used for compact EV/renewable designs, higher frequencies, and >99% efficiency.
- 2) Digital/AI controllers using DSPs for load balancing and adaptive, real-time THD reduction in interleaved topologies.
- 3) By 2035, there will be a \$4 billion or more market for smart grids, solar inverters, and rapid chargers in order to comply with tougher IEC regulations.

For dynamic compensation, a hybrid PFC with SVG reduces losses in fluctuating loads by 20–30%.

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