An Energy-Efficient Single-Phase TC-UPQC Featuring Optimized DC-Bus Allocation

GUGULOTH SONIYA [1]|M.RAGINI [2]
[1]PG SCHOLAR, Dept of. ELECTRICAL POWER SYSTEM, Avanthi Institute of Engineering and Technology (AUTONOMOUS), Ts, India.
[2]ASSISTANT PROFESSOR, Dept of Electrical and Electronics Engineering, Avanthi Institute of Engineering and Technology (AUTONOMOUS), Ts, India.

ABSTRACT: To control grid current and stabilize load voltage, a unique single-phase transformerless three-capacitor unified power quality conditioner (TC-UPQC) is suggested. It is made up of one buffer capacitor and two active capacitors. One active capacitor is used to withstand variations in grid voltage, while the other is connected in series with a buffer capacitor to provide current compensation. Internal half-bridge voltage-source converters (VSCs) control the voltages of active capacitors, while the buffer capacitor handles the residual voltage imposed by the load voltage. As a result, better modulation degrees could be achieved and the magnitude difference between the two active capacitor voltages could be reduced. Additionally, lowering the active capacitor voltages could significantly lower the dc-link voltage. In line with this, power balance control is suggested for coordinating VSC operations and controlling dc-link voltage. In order to provide operational flexibility even in the absence of an external bi-directional dc power supply, active power is incorporated into voltage and current compensation. The efficacy of the suggested TC-UPQC is confirmed by simulation platforms.

KEYWORDS: TC-UPQC, VSC, BUFFER CAPACITOR, GRID.

I.INTRODUCTION: Unified energy nice conditioners (UPQCs) had been essential to grid balance and dependability in latest decades. To enhance power great in distribution structures, it incorporates shunt and collection lively electricity filters (APFs) [1], [2]. The distribution line between the utility grid and the burden is connected in collection with the series active filter out, additionally known as a dynamic voltage restorer (DVR) [3], [4]. In order to make sure that the load gets a steady and controlled voltage despite fluctuations inside the software deliver, it video display units the voltage waveform and injects compensating voltages to reduce sags and swells. The distribution line and the shunt active filter, additionally called an APF, are linked in parallel at the factor of not unusual coupling [5], [6]. In order to reduce harmonics, reactive electricity, and voltage distortions added on by nonlinear masses, it keeps a watch on the modern waveform and injects compensatory currents. The distribution gadget's overall harmonic distortion (THD) is decreased and strength thing correction is stepped forward via the APF. To guarantee clean operation and thorough power first-class monitoring, DVR and APF are related back-to-lower back thru a DC connection and coordinated by a single control machine. Depending on unique grid situations and energy quality requirements, UPQC architecture may be modified and optimized. Single-segment UPQCs provide flexible methods to decorate electricity first-rate in a diffusion of applications, from business and renewable energy integration to residential and business settings [7], [8].

Because it may prevent short circuit issues and provide voltage regulation, isolation, and impedance matching abilties, the mixing of line-transformers with UPQCs has drawn quite a few interest [9]. However, line-transformers are usually high priced and large parts that limit the strength density of the converter and add volume, weight, and losses. These shortcomings brought about researchers to look for several transformerless UPQCs. High-frequency transformers can decrease size, value, and losses whilst keeping off the problems of line-transformers [10]. Multilevel UPQCs, which are examined in [11], [12], [13], and [14], appear like an intriguing opportunity to satisfy the best requirements whilst excessive-frequency transformers are inserted and coupled in collection with the grid deliver. Multilevel UPQCs perform higher than -stage converters in terms of energy pleasant, performance, low-voltage stress, smaller output filters, and elevated energy range functionality. But in reality, those topologies transfer electricity using returned-to-again topology. Low performance is the result of all of the energetic power passing thru the converter. Furthermore, extra semiconductor switches are required for multilevel UPQCs with excessive-frequency transformers, which increases the converter's value.

Transformers may be effectively replaced via active capacitors. Based in this, a unmarried section, four-leg nonisolated UPQC made up of two separate H-bridge converters connected lower back-to-returned changed into proposed through Because UPQC series and shunt converters commonly have the identical frequencies, DVR and APF can use a shared bridge arm. This results in the application of three-leg UPQC as illustrated in Fig. 1(a). This configuration requires fewer semiconductor switches than. However, mutual coupling is delivered with the aid of the identical bridge arm among collection and parallel converters. Controlling contemporary harmonics and maintaining load voltage are made greater difficult by means of this mutual coupling. Series capacitors can be utilized in location of shared legs in three-leg UPQC to in addition lessen the quantity of semiconductor switches. Because of this, the two-leg UPQC depicted in Fig. 1(b) is changed and called GHLF UPQC, with grid parallels to the half-bridge shape and load parallels to the full-bridge shape. Two-leg UPQC in this topology calls for simplest four semiconductor switches, that is economical.

However, another bothersome trouble for three-leg or 4-leg UPQC primarily based on complete-bridge converters is leakage present day that appears within the converter because of the lack of a line-transformer. However, because a half of-bridge creation is intended for DVR and APF, leakage modern can be correctly reduced in -leg UPQC. In -leg UPQC, switching devices are subjected to high voltage traces due to the fact the dc-hyperlink voltage have to be extra than two times the height grid voltage when the grid is related to the ac output of a half of-bridge converter. Another more suitable -leg UPQC, called GFLH UPQC, is illustrated in Fig. 1(c) as grid parallels to the full bridge shape and load parallels to the 1/2-bridge structure in order to eliminate the twice dc-hyperlink voltage constraint added on by using the half-bridge converter. Since UPQC's APF is a complete-bridge converter, the dc-link voltage just desires to be better than the grid voltage top. However, because the GFLH UPQC load is connected because the half-bridge converter's ac output, the dc-link voltage should be extra than twice the height load voltage, which raises the dc-link voltage in a comparable way. Nevertheless, during grid swell, the dc-link voltage in GFLH UPQC might be lower than GHLF UPQC.

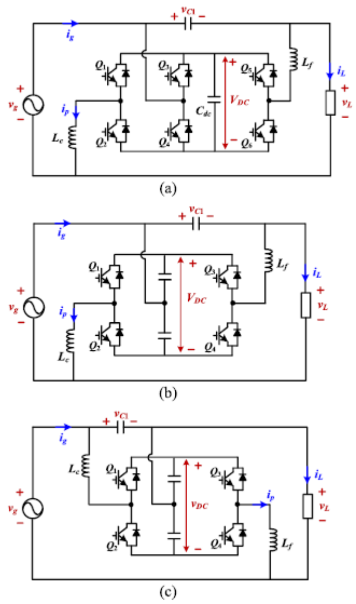


Fig. 1. Conventional single-phase transformerless UPQCs. (a) Three-leg UPQC. (b) GHLF UPQC. (c) GFLH UPQC.

II.PROPOSED SYSTEM: In two-leg UPQC, switching devices are subjected to high voltage strains because the dc-link voltage must be greater than twice the peak grid voltage when the grid is linked to the ac output of a half-bridge converter. Another enhanced two-leg UPQC, called GFLH UPQC, is illustrated in Fig. 1(c) as grid parallels to the full bridge structure and load parallels to the half-bridge structure in order to eliminate the twice dc-link voltage constraint brought on by the half-bridge converter. Since UPQC's APF is a full-bridge converter, the dc-link voltage just needs to be higher than the grid voltage peak. However, because the GFLH UPQC load is connected as the half-bridge converter's ac output, the dc-link voltage must be greater than twice the peak load voltage, which raises the dc-link voltage in a similar manner. Nevertheless, during grid swell, the dc-link voltage in GFLH UPQC may be lower than GHLF UPQC. According to IEEE 1453-2022, grid voltage fluctuations are typically less than 10% of the grid voltage amplitude. The ac output voltage magnitude in DVR is significantly smaller than that in APF in current nonisolated topologies. Additionally, APF and DVR share a same DC bus. The switching harmonic proportion increases as a result of DVR operating at a very low modulation degree. As a result, the converter's efficiency will be reduced by needless switching loss of DVR brought on by excessive dc-link voltage. As illustrated in Fig. 2, a unique single-phase nonisolated three-capacitor UPQC (TC-UPQC) is presented to shield dc-link voltage from the constriction of external ac output voltages (e.g., grid voltage, load voltage) and achieve superior modulation degrees. It is made up of one buffer capacitor and two half-bridge voltage source converters (VSCs). The APF of TC-UPQC is formed by connecting one converter (VSC.1) as a DVR and another (VSC.2) in series with a buffer capacitor. Active capacitor C2 receives a tiny amount of the load voltage, while buffer capacitor C3 receives the rest voltage. As a result, higher modulation degrees could be obtained and the magnitude difference between active capacitor voltages could be reduced. Additionally, a lower dc-link voltage could be achieved by reducing the maximum value of two active capacitor voltages.

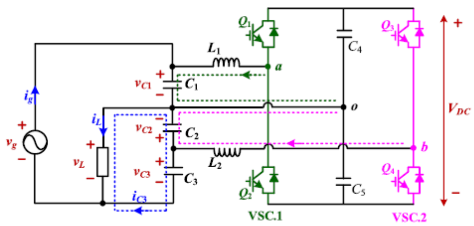


Fig. 2. Proposed TC-UPQC.

In conclusion, the following are the study's primary contributions. 1) To prevent grid voltage flickering, increase grid-side power factor, and improve grid current quality, a unique single-phase transformerless TC-UPQC is first presented. 2) The magnitude difference between two active capacitor voltages is reduced when the buffer capacitor can withstand a substantial proportion of the ac source voltage. Superior modulation degrees could therefore be created for VSCs, which is advantageous for improving efficiency and switching harmonic suppression. 3) The dc-link voltage is significantly lowered as the maximum value between two active capacitor voltages decreases. Therefore, using fitting power electronic components (such as electrolytic capacitors and semiconductor devices) might make the design of UPQC more economical. 4) A power-balanced technique is suggested to coordinate VSC operations. Therefore, by trading active power with external circumstances, the voltage or current compensation might be more adjustable. However, in the absence of an external bi-directional DC power supply linked to the DC bus, the DC-link voltage could remain steady.

The circuit description, dc-link voltage specifications, load-side voltage compensation, grid-side current compensation, and harmonic distortion mitigation of the proposed TC-UPQC are all covered in detail in this section. Buffer capacitor C3, VSC.1 (leg a: switches Q1, Q2; leg o: dc-link capacitors C4 and C5; filter: inductor L1, capacitor C1), and VSC.2 (leg b: switches Q3, Q4; leg o; filter: inductor L2, capacitor C2) are the three primary components of the proposed TC-UPQC, as seen in Fig. 2. Leg o is shared by VSC.1 and VSC.2. Grid voltage, grid current, load voltage, and load current are represented by the symbols vg, ig, vL, and iL. The voltages of C1, C2, and C3 are represented by the symbols vC1, vC2, and vC3, and the currents passing through them are represented by the symbols iC1, iC2, and iC3. The dc-link voltage is represented by the symbol VDC. Three current loops are indicated by dashed lines of various colors to show how TC-UPQC works. With active capacitor C1 controlled by VSC, Loop 1 (green dashed line) is pertinent.1. With active capacitor C2 controlled by VSC, Loop 2 (magenta dashed line) is pertinent.2. With buffer capacitor C3 connected in series with VSC, Loop 3 (blue dashed line) is pertinent.2. TC-UPQC has three duties to finish. First, the load voltage and grid current should have a sinusoidal shape. Grid voltage vg, grid current ig, and load voltage vL could be expressed as follows if grid voltage is unpolluted:

$$\begin{cases} v_g(t) = V_g \cdot \sin(\omega t) \\ i_g(t) = I_g \cdot \sin(\omega t + \varphi_g) \\ v_L(t) = V_L \cdot \sin(\omega t + \delta) \end{cases} \quad (1)$$

where ϕg is the grid-side power factor angle and ω is the power grid's angular frequency. The phase difference between grid voltage vg and load voltage vL is represented by the symbol δ. The peak values of grid voltage vg, grid current ig, and load voltage vL are represented by the symbols Vg, Ig, and VL. Second, the grid voltage and current must be in phase. Therefore, by supplying an appropriate compensatory current, phase angle ϕg should be adjusted to zero. Third, it is necessary to control the load voltage vL to a standard value. The standard value of VL (the magnitude of load voltage vL) is represented by the symbol V ∗ L. The difference between V ∗ L and Vg is represented by the symbol ΔVg.

$$\Delta V_g = V_g - V_L^*. \quad (2)$$

ΔVg > 0 if the grid swells. ΔVg < 0 if the grid swags. Therefore, by supplying an appropriate compensating voltage, vL might be controlled to V ∗ L. The similar model is shown in Fig. 3(a) to demonstrate how TC-UPQC operates. Between the grid and the load voltage, VSC.1 functions as a controlled voltage source (vC1). It is possible to control the load voltage vL to be sinusoidal with a constant magnitude by altering the series voltage vC1. The following time-domain formula accomplishes this.

$$v_{C1}(t) = v_g(t) - v_L(t). \quad (3)$$

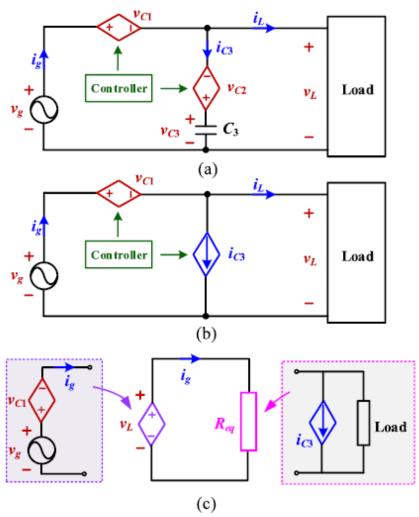
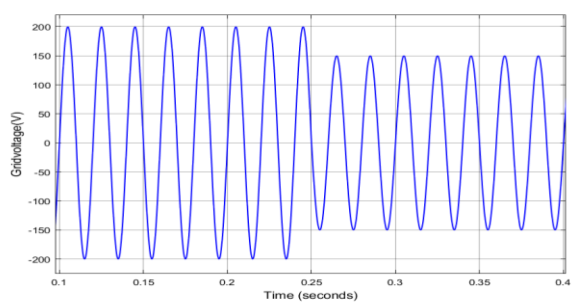


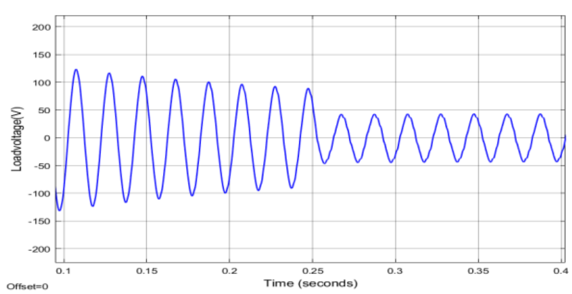
Fig. 3. Equivalent model of the proposed TC-UPQC. (a) Step 1. (b) Step 2. (c) Step 3.

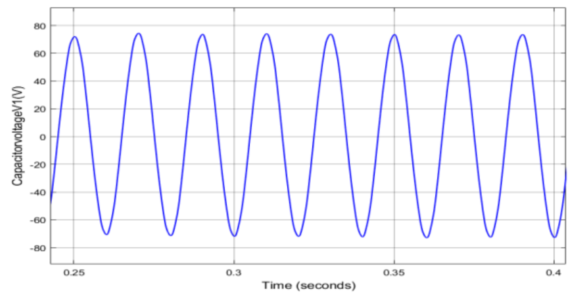
Furthermore, sufficient compensatory current must be provided to counteract the reactive current and harmonic current caused by the load. Kirchhoff current law could be used to obtain fitted compensatory current iC3.

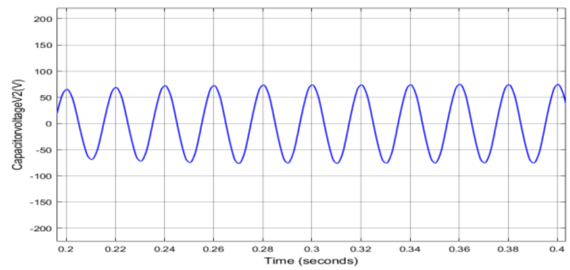
$$i_{C3}(t) = i_g(t) - i_L(t).$$

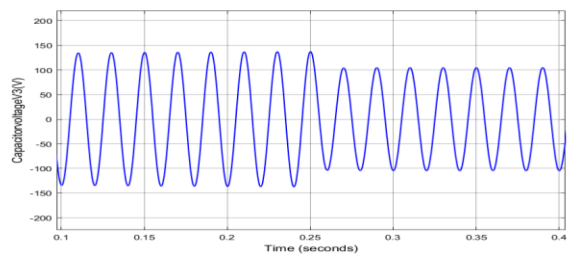
III.SIMULATION RESULTS:

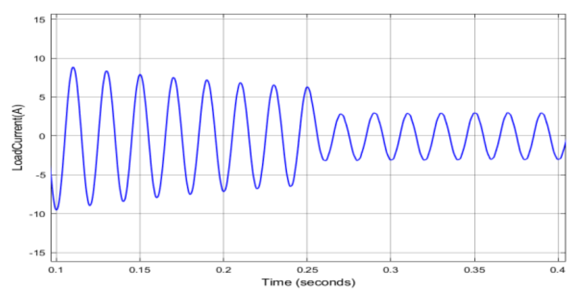


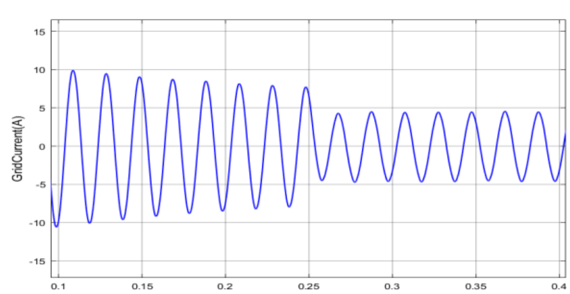


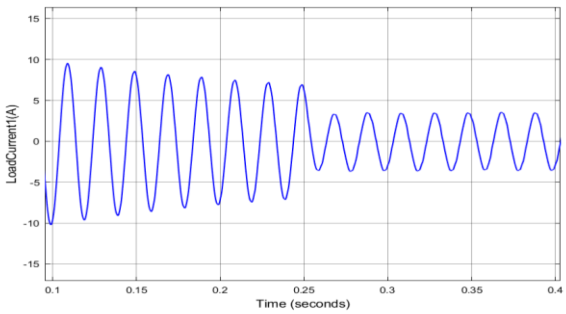


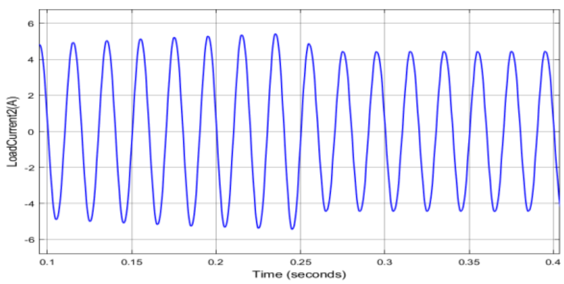




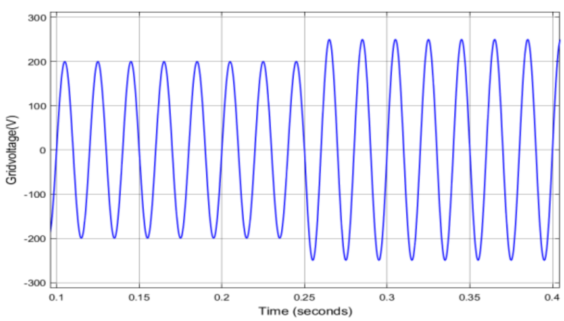


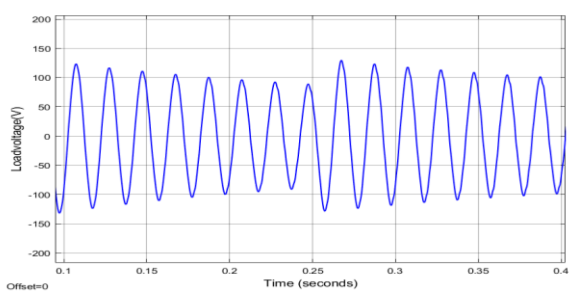


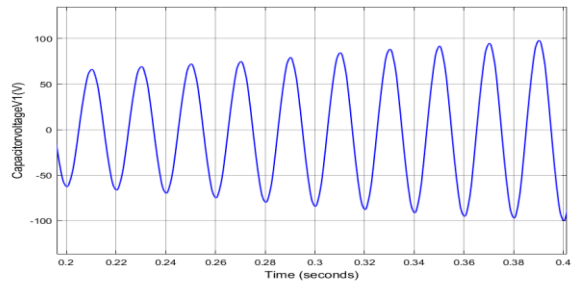


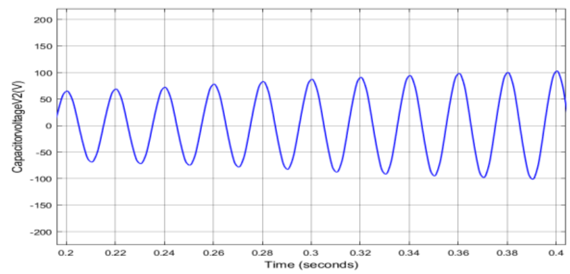


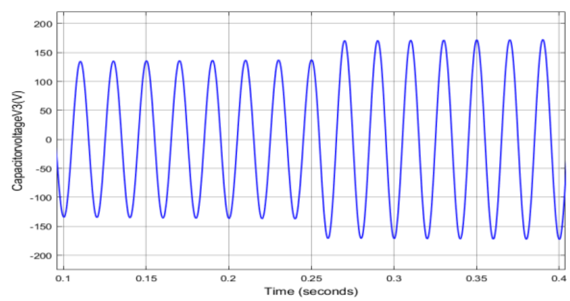
Case2 swell condition

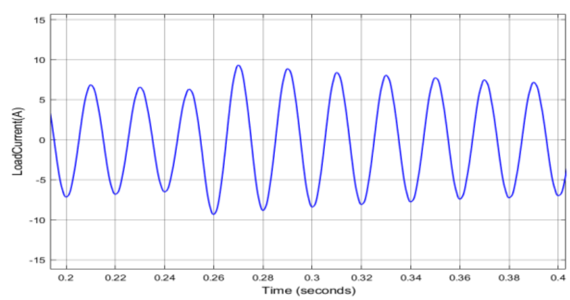


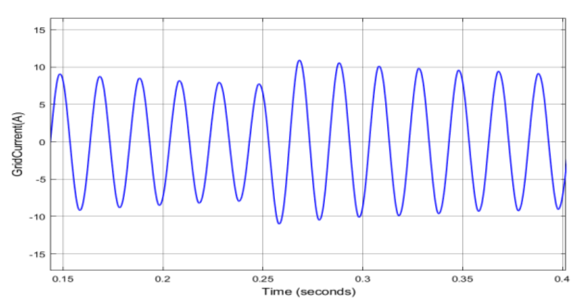


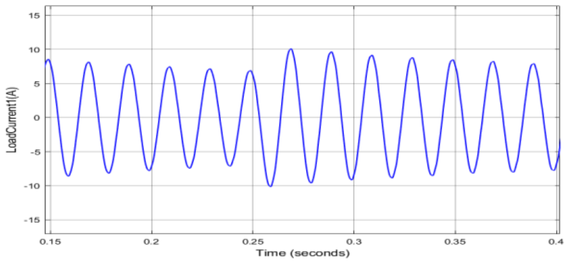


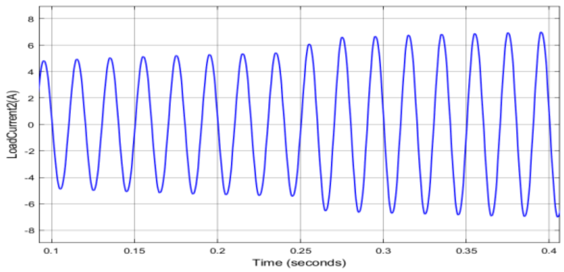


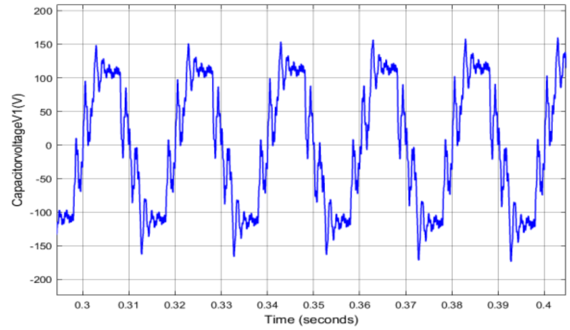


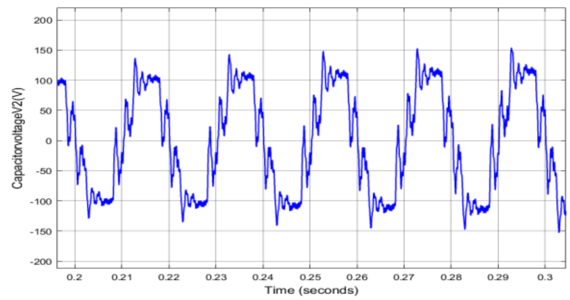




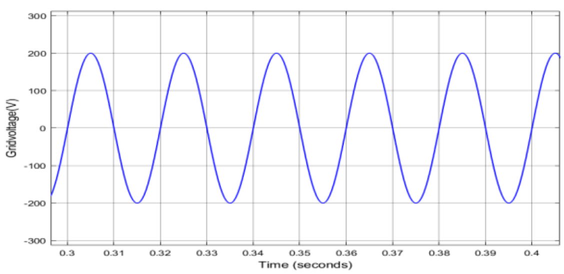


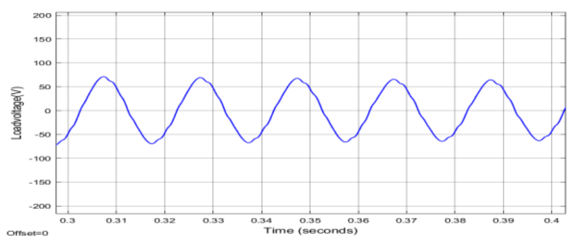


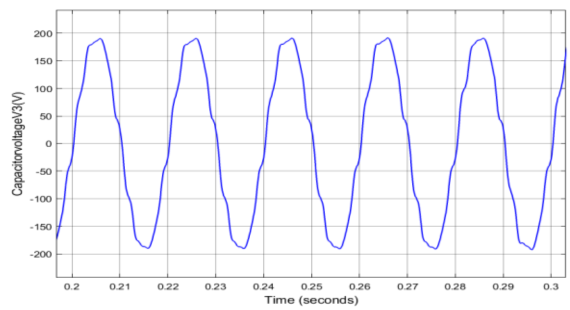


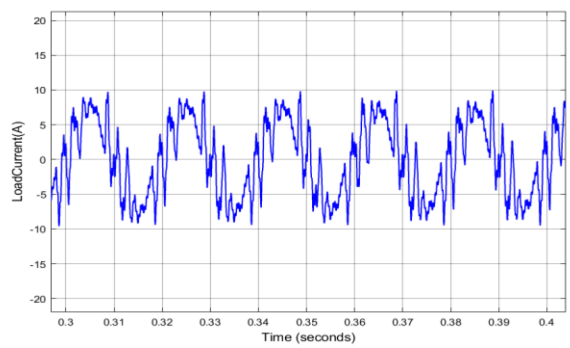


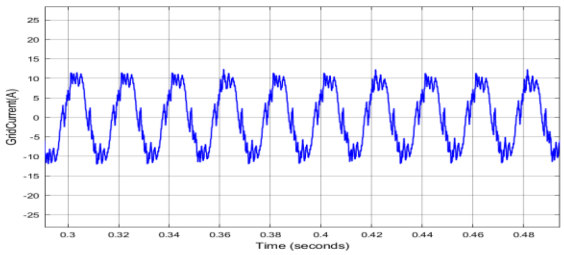
Case3 Nonlinear load











IV.CONCLUSION: To reduce dc-link voltage and achieve the ideal modulation degrees, a single-phase nonisolated TC-UPQC is suggested. Two active capacitors and one buffer capacitor are part of this arrangement. Grid voltage sag/swell is compensated for by one active capacitor, while current compensation is handled by the other active capacitor in conjunction with the buffer capacitor. While the buffer capacitor controls the remaining voltage from the grid, internal half-bridge VSCs control the voltages of the active capacitors. By reducing the ratio of active capacitor voltages to grid voltage, this design dramatically lowers the dc-link voltage. To manage the dc-link voltage and synchronize the VSCs' operations, a power balance management technique is also presented. This method improves operating flexibility even in the absence of an external bi-directional dc power supply by integrating active power into both voltage and current correction. Simulation confirms the accuracy of the associated power balance control approach and the efficacy of the suggested TC-UPQC.

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