Design and Implementation of Low Power Area efficient Master Slave Flip-Flops

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ABSTRACT

A Conventional edge triggered master-slave flip-flop is very sensitive to particle that causes an error. Master latch upsets the logic state with an error, when the clock signal is high where as the slave latch upsets the logic state when the clock signal is low, resulting in an erroneous output of the flip-flop. Here in this paper a new flip flop is presented which can overcome or control any type of error. Here the terms error, single event upset(SEU) and soft errors represent the same meaning. We use an error detection circuit which is used to detect errors and a multiplexer for generating fault indication signal. An error in the master latch or slave latch can be detected when the clock signal is high or low using error detection circuit. The correct output is being generated by the multiplexer using error indication signal, for more efficient results an n-type pass transistor followed by an inverter was introduced instead of transmission gates. The proposed ff with multiplexer and transmission gate and ff with multiplexer and n-type pass transistors have small area, less power dissipation and delay overheads.

Keywords: Flip-flop, hardened techniques, SEU (soft error), Multiplexer, N-type pass transistor.

INTRODUCTION

As VLSI circuits goes on with the evolution and technologies progress, the level of integration is increased and we can achieve high clock speed. Higher clock speeds, increase in levels of integration and scaling of technology are the reasons for the increase in power consumption. As a result, low power consumption has become a serious issue for modern VLSI circuit implementation. Moreover, performance of transistor has limited the power dissipation, static and dynamic for long term device reliability, and increase in integration. Flip-flop is a data storage element. The operation of flip-flops is done by the clock frequency. When multistage flip-flop is operated with respect to the clock frequency, it goes on with high clock switching activity and then increases latency of time. Therefore the speed and energy performance of circuit is affected. To achieve high-speed and low energy operation various flip-flop classes were proposed. To achieve low power dissipation along with area, a new flip-flop with less number of transistors is being proposed and compared with the conventional flip-flop.

POWER DISSIPATION

Power dissipation is one of the crucial parameter in the modern VLSI design field. We require consideration for peak power consumption for the design of small devices to ensure performance and proper operation. There are four sources of power dissipations. They are switching power, leakage power, static power and short circuit power.

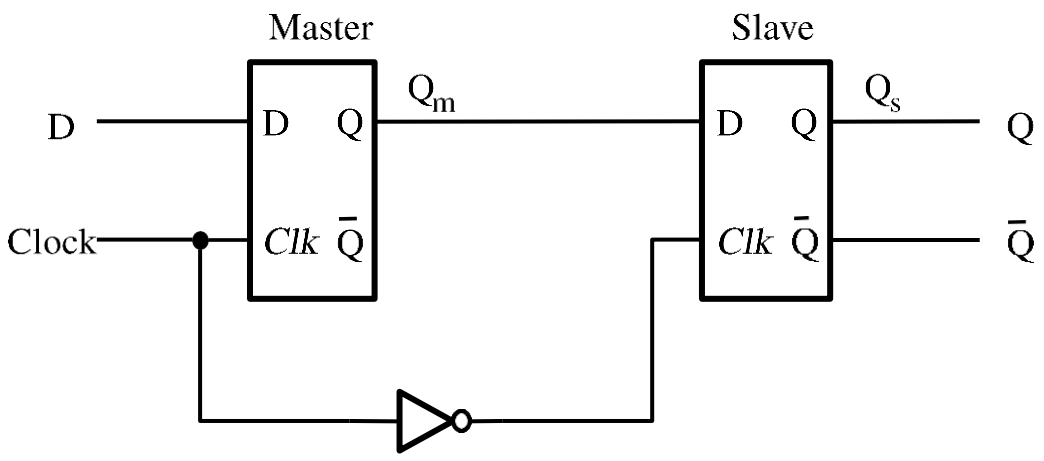
Y. Cao, “New paradigm of predictive mosfet and interconnect modeling for early circuit design,” in Proc.Custom Integrated Circuits Conf., Orlando, FL, USA, 2000, pp. 201–204.

Feature size scaling and reduction of operating voltages, chips became too sensitive. So, latches and flip flops are susceptible to single event upset(SEU)[1]. These SEU’s are also known as soft errors and these leads to incorrect output. Strike of particle may affect both ff and latches sensitive, which may cause error. FF or latch logic state may be upset during the hold time and these are corrected when a new value is written into it. Single event upset or soft error is nothing but change of state which strikes a particle in electronic devices such as microprocessor, power transistor or semiconductor memory.

C. E. Stroud, “Rel. of majority voting based VLSI fault-tolerant circuits,” IEEE Trans. Very Large ScaleIntegration (VLSI) System, vol. 2, no. 4, pp. 516–521, 1994.

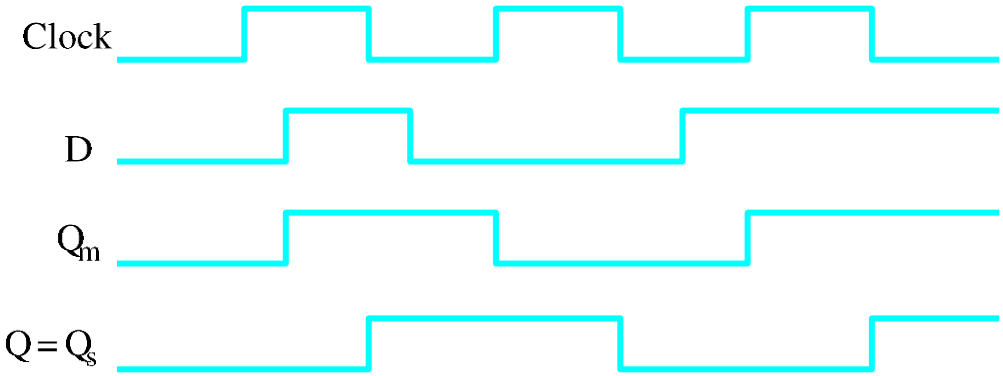
MASTER-SLAVE EDGE-TRIGGERED FLIP-FLOP

In the master slave edge-triggered flip-flop, master can connect two level sensitive latches to catch the value of the input “D” at Q- when ck signal is low. Slave latch causes change in clock signal, Q at rising edge.

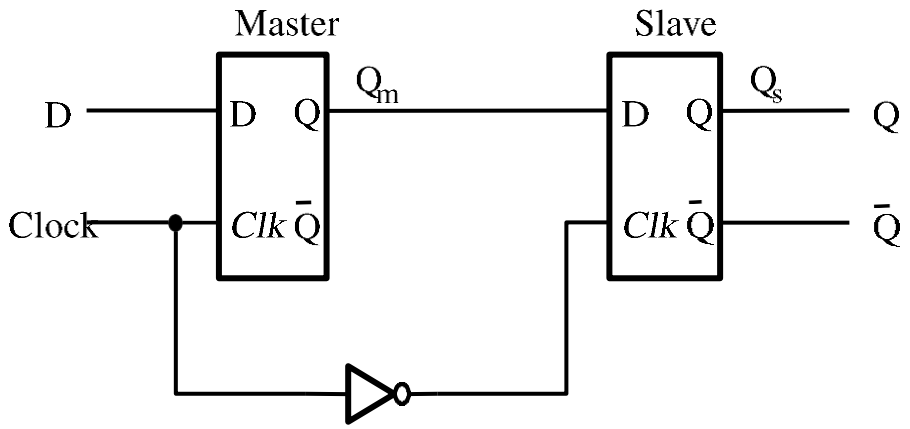


A rising edge is the low -to -high transition. It is also known as positive edge. In the rising edge-triggered the circuit becomes active at low- to -high transitions of clock signals, and avoids the high-to-low transition. A falling edge is reverse case where it is the high- to –low transition. It is called as the negative edge and this avoids low- to- high transitions.

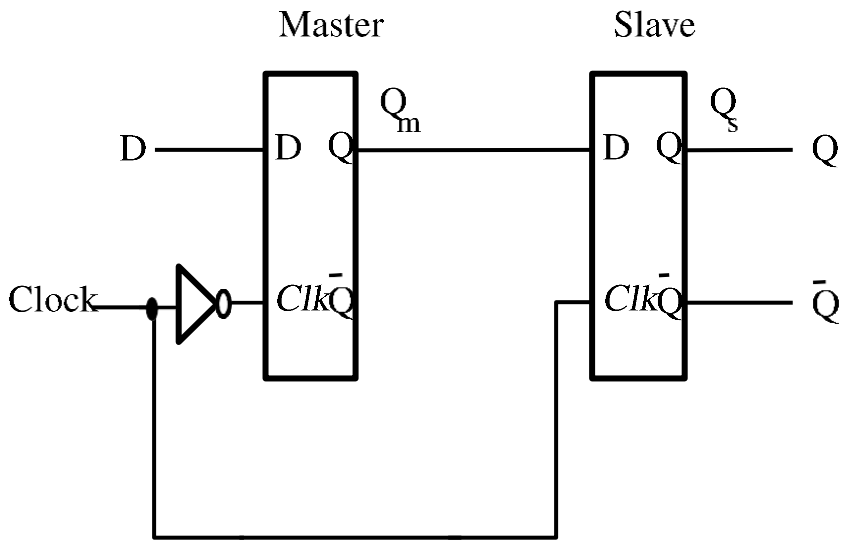
Timing Diagram for the Master-Slave D Flip-Flop:



Negative-Edge-Triggered Master-Slave D Flip-Flop:



Positive-Edge-Triggered Master-Slave D Flip-Flop:



CONVENTIONAL RISING EDGE TRIGGERED FLIP FLOP

We know that a conventional master slave ff operates when an input given to the master latch, it stores the value and the clock signal transition to the slave latch and generates the output same as the input. In case any error occurs the output may not follow the input. Here in the below circuit there exists fault in the output for which we are going to introduce error detection circuit.

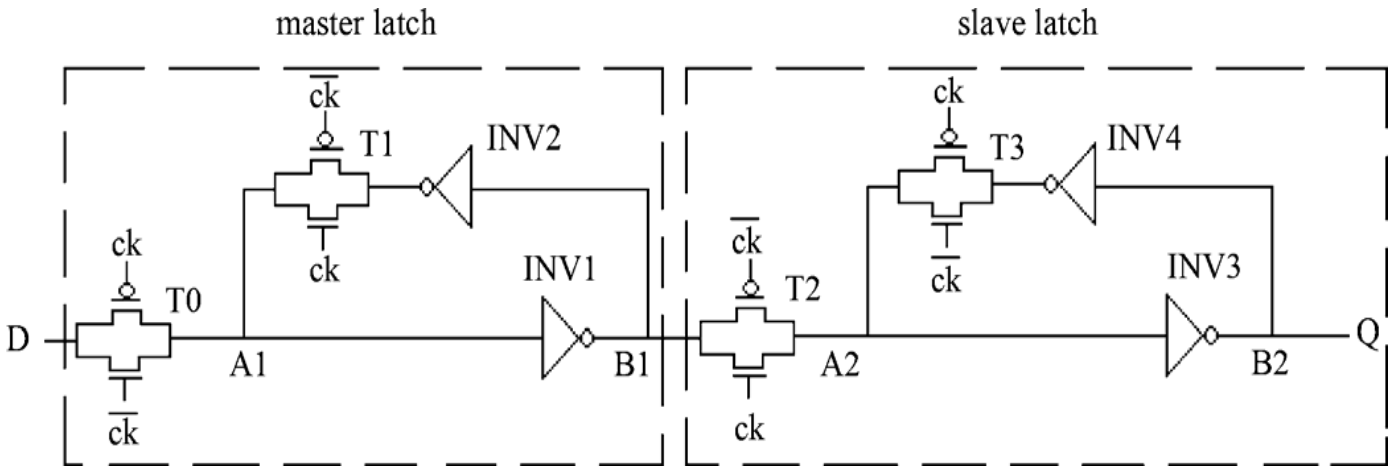


Figure 1: Conventional master slave flip flop

In the below wave forms we can observe the output is faulty as it is exactly the inversion to its input. So modifications must be made for producing error free output.

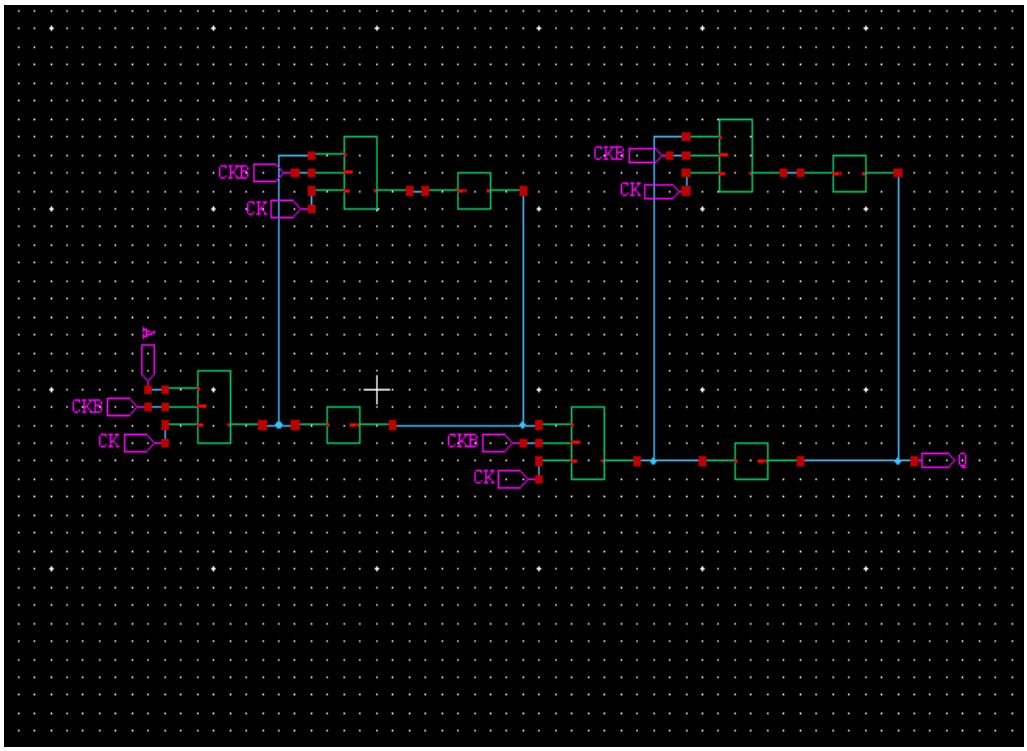


Figure 2: Conventional master slave flip flop

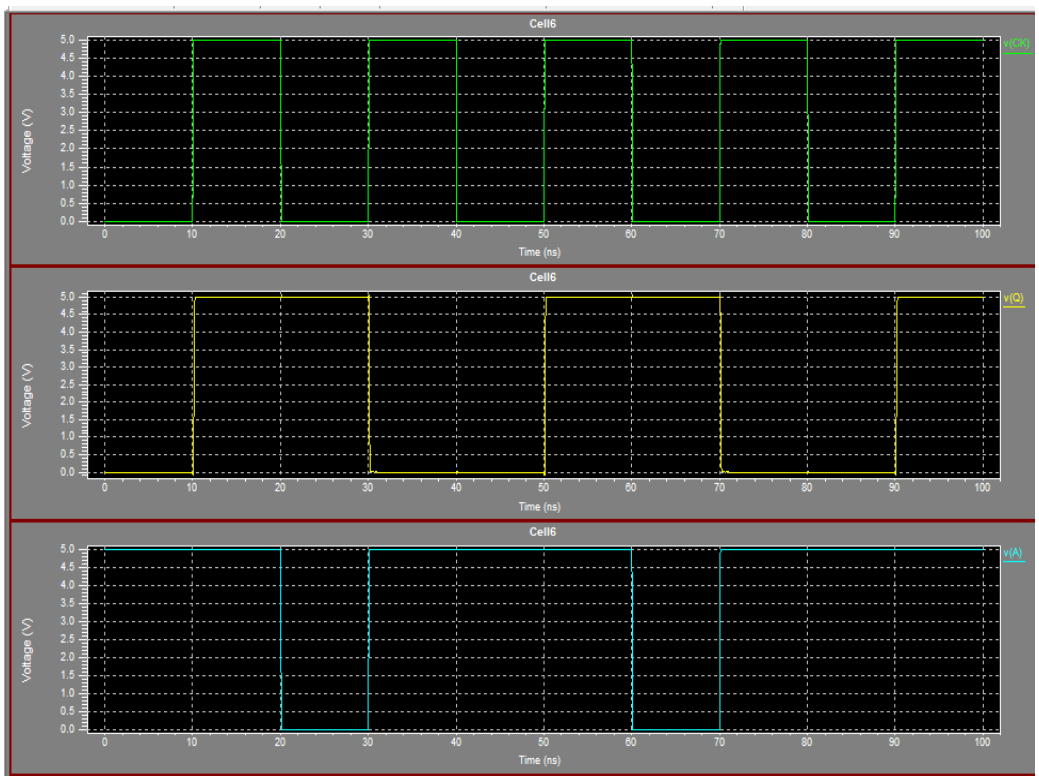


Figure 3: Waveforms of conventional master slave flip flop

EXSITING SEU HARDENED FLIP-FLOP.

The proposed error hardened ff uses error detection circuit which consists of two inv, XNOR gate and a NAND gate with some transistors. This is used to detect errors in the master latch and slave latch. Multiplexer uses fault indication signal, which is indicated by S, to select the correct output. The NAND gate produce logic

1, when the clock signal is low and where as produces logic 0, when the clock signal changes from low -to -high during its transition period. When the signal S is pre-charged to logic 1, M1 is turned ON in PMOS, M3 is turned OFF in NMOS. When signal is pre-charged to logic 1, the output values at Q via multiplexer . After rising edge the NAND gate returns to output logic 1 when the clock signal is high. In the reverse case when M1 is OFF in PMOS and M3 is ON in NMOS, the signal selects node Q as final output due to open NMOS M2 at logic 1.

D. R. Blum and J. G. Delgado-Frias, “Delay and energy analysis of SEU and SET-tolerant pipeline latches and flip-flops,” IEEE Trans.Nucl. Sci., vol. 56, no. 3, pp. 1618–1628, Jun. 2009

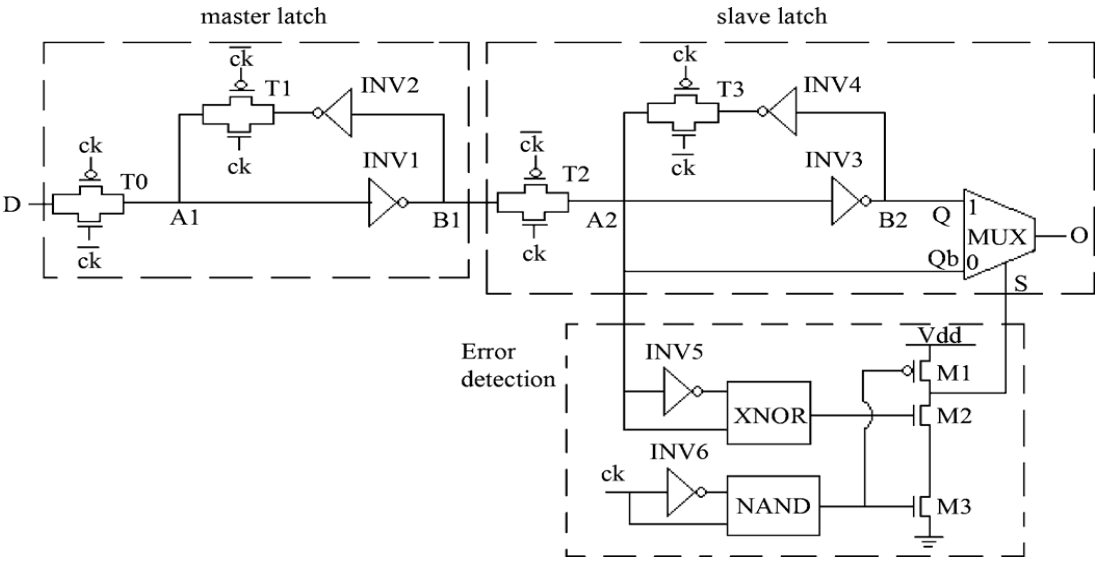


Figure 4: Conventional master slave flip flop with multiplexer

The transmission gate is ON for node A1, 0 TO 1 FOR NODE b1, 1 to 0 for node A2. If any difficulty arises it is corrected by the XNOR gate having logic 1 during its invalid transition period. NAND gate produces logic 1, when the clock signal is low. If no error occurs when the clock signal is high, the node Q is selected as final output at logic 1. If any error affects the error detection circuit Qb is selected as final output at logic 0. If the erroneous transition affects the multiplexer 0 is selected as the final output and it may be erroneous output.

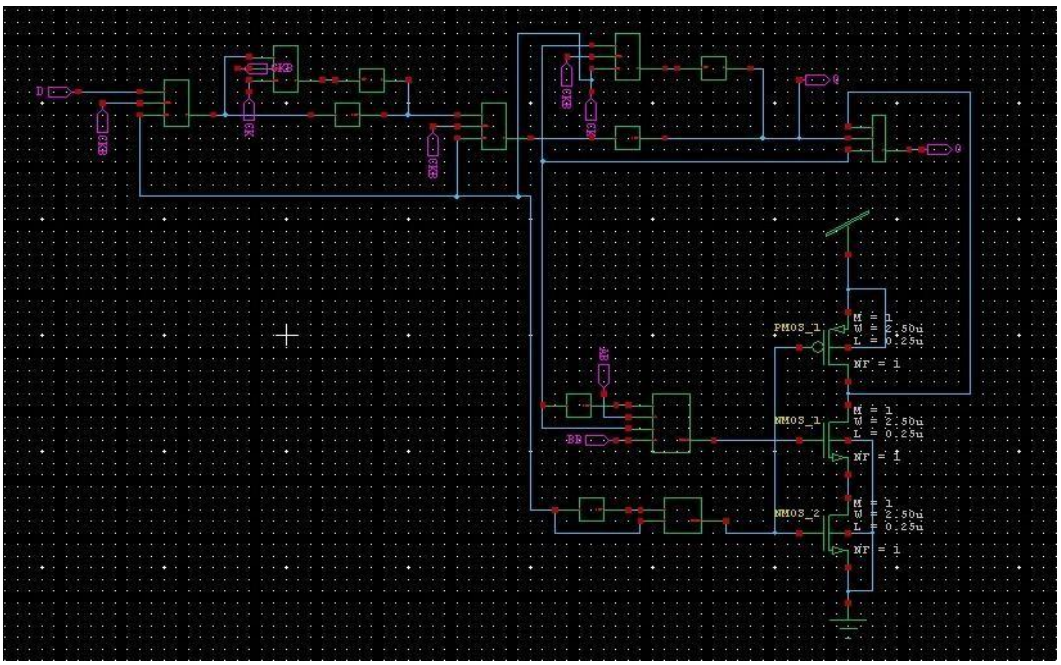


Figure 5: Existing SEU flip-flop

The waveforms obtained for this conventional master slave ff along with the simulation process were as follow

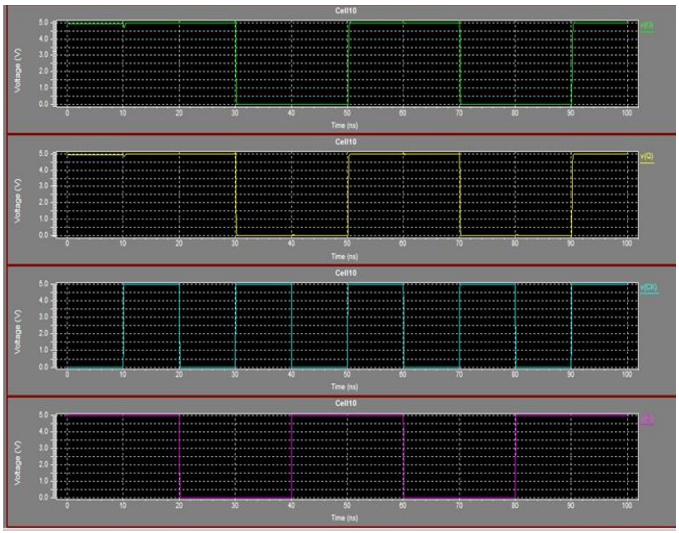


Figure 6: Waveforms of conventional master slave flip flop

POPOSED FLIP-FLOP SCHEMATIC

Here we can replace the modified n-type pass transistor ff in place of the conventional ms D ff. The power and area are compared with the existing system. During hold phase, master slave logic state may upset at node A1 or B1 in the faulty output Q. when the clock is low, it locks the erroneous value. Whereas during Z the hold phase , the slave latch upsets the results in faulty output Q at node A2 or B2. During the whole clock signal period , the error hardened ff can overcome errors. The error indication signal selects Qb as final output at exact value. Here this ff produces small area and less power dissipation.

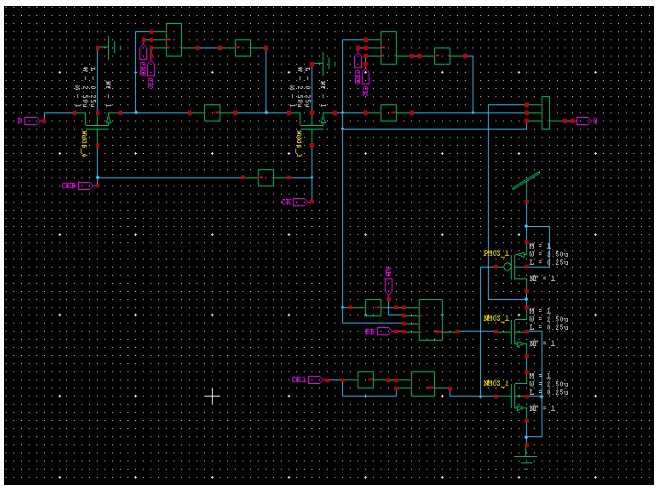


Figure 7: n-type pass transistor

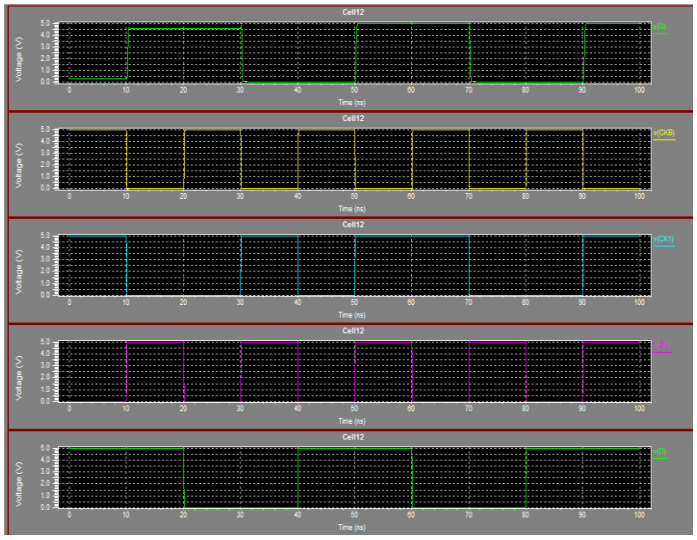


Figure 8: Waveforms of proposed flip flop

APPLICATION

Asynchronous Counter is generally not used in HF counting circuits were large numbers of bits are involved. Also, the outputs from the counter do not have a fixed time relationship with each other and do not occur at the same instant in time due to their clocking sequence. In other words the output frequencies become available one by one, a sort of domino effect. Then, the number of ff that are added to an asynchronous counter chain the lower the max operating frequency becomes to ensure accurate counting. To overcome the problem of propagation delay Synchronous Counters were developed.

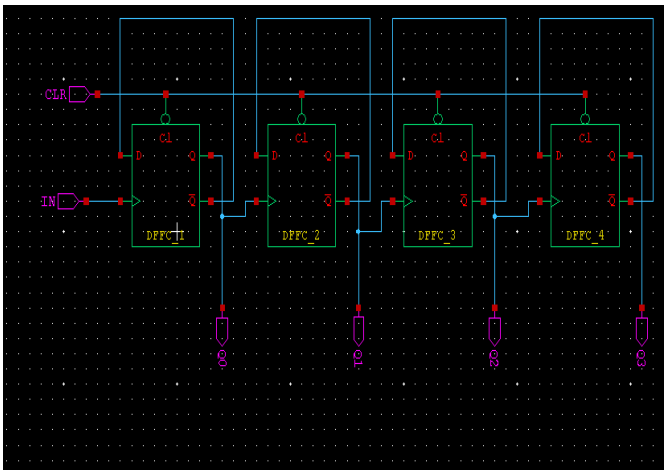


Figure 9: Asynchronous counter

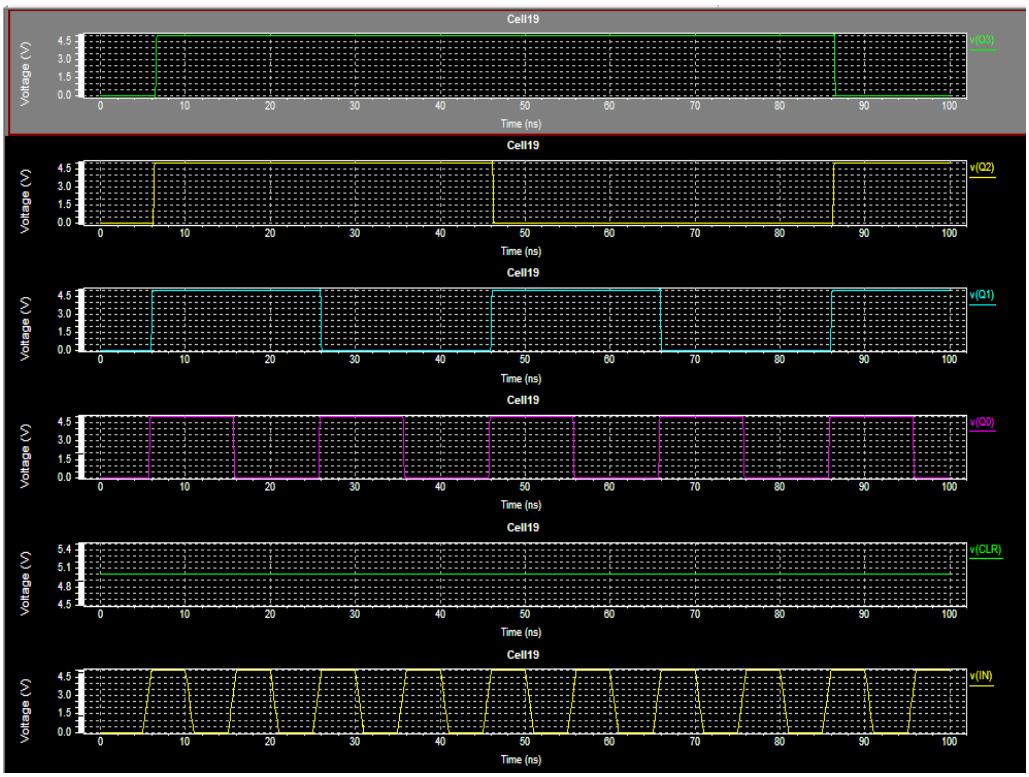


Figure 10: Waveforms of asynchronous counter

SIMULATION

To compare the performance of proposed ff with existing ff designs, all the circuits are designed using Tanner tools schematics and layout editor and extracted using 250nm CMOS technology [7]. Simulations were carried using T-spice. This ff is simulated with the supply voltage of 5V.

Flip-Flops	No. Of transistors	Rise time	Fall time	Power dissipation
Conventional master slave flip-flop	24	301.21ps	181.9ps	31.4nw
Flip-flop with multiplexer and transmission gates	49	141.23ps	112.8ps	21.6nw
Flip-flop with multiplexer and n-type pass transistor	39	141.86ps		

From the above table, number of transistors and power dissipation of the ff using multiplexer and n-type pass transistors is observed to be less when compared with the ff using multiplexer and transmission gate. And number of transistors and power dissipation for the new ff proposed is observed to be less in comparison with the conventional ms ff.

CONCLUSION

New less area and low power consumed ff are proposed using multiplexer and transmission gates and ff using multiplexer and n-type pass transistors. The proposed ff was compared with the conventional flip-flops and seems to be exhibiting low power dissipation and less area occupation. The proposed ff using multiplexer with transmission gate and ff with multiplexer and n-type pass transistors results in reduction in the power dissipation up to 50-60% and area up to 30-50% in comparison with the conventional ff. The asynchronous counter designed with proposed ff using multiplexer and transmission gate and ff using multiplexer and n-type pass transistors exhibits power dissipation reduction. Hence the proposed architectures demonstrates less area and low power dissipation in the circuit where delay overheads.

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