LOW-POWER HIGH-SPEED SENSE-AMPLIFIER- BASED FLIPFLOPS WITH CONDITIONAL BRIDGING

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Abstract: One of the major challenges in modern VLSI design is power consumption, right up there with space and performance. Digital systems rely on the flip-flop. In sub-threshold operation, we examine and contrast four different flip-flop topologies: IP-DCO, MHLFF, CPSFF, and CPFF. Both pulse-triggered and conditional approaches are included in these topologies. Very low power consumption applications are now within reach, thanks to sub threshold technology. One advantage of this technique is that it decreases the number of power-hungry flip-flops. Compared to a strong inversion circuit, a subthreshold circuit consumes less power while running at the same frequency. Tanner uses 18nm technology in cmos for design. We test the flip-flops' power delay, power delay product, and average power at a 1V power supply voltage and look at them from every perspective.

Keywords: Sub Threshold Technology, Flip Flop, Low Power.

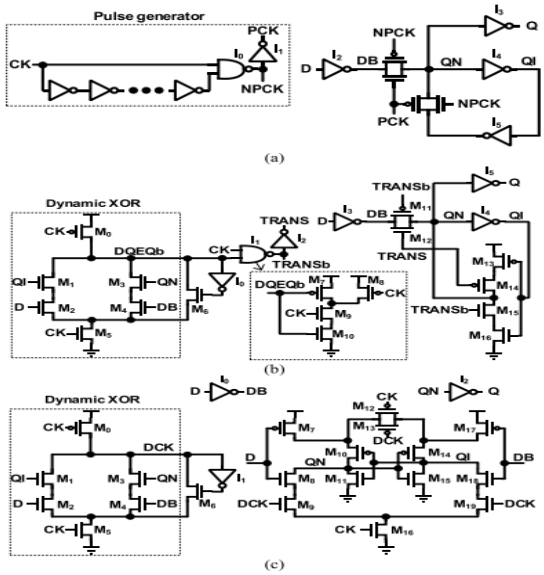
1. INTRODUCTION

To satisfy the need for electronic systems to function at high speeds, clock frequency increases and tighter timing requirements are required [1]. These systems have used high-speed circuits, which consume a lot of power, to satisfy the required timing standards. The need for computations that are energy efficient has grown in recent times due to the widespread use of mobile electronic devices in daily life [2, 3]. Energy constraints may be addressed using low-power design solutions, which may involve sacrificing speed performance. These tactics include voltage scaling to decrease switching power and conditional operations to prevent redundant power [4, 5]. Making a conscious effort to reduce power consumption in order to achieve quicker processing speeds is standard practice for high-performance mobile applications. Digitally integrated systems that are in sync use flip-flops

and latches to control state transitions and synchronised data flow. Since flip-flops are often used in timing-critical signal pathways, which dictate the maximum working frequencies, their high-speed design is vital [8]. With millions of flip-flops used by a single processor and their combined power consumption exceeding 20-40% of the total power, low-power flip-flop design has become more important in recent years [9], [10], [11]. Since it is not possible to simultaneously reduce power consumption and delay caused by flip-flops and latches, this becomes an essential consideration in the design of high-speed mobile electronic systems. With its master-slave architecture, the transmission-gate flip-flop (TGFF) [12] (FIGURE 1) may provide synchronous digital integrated circuits minimal power consumption and data-to-output (DQ) latency. Another potential benefit of TGFF's reliable operation in the near-threshold voltage (NTV) range is power savings via voltage scaling. By dividing the sampling and capturing of input data into the master and slave phases, respectively, so-called pulse-based techniques in TGFF may decrease the DQ latency [13], [14], [15]. A pulse generator and one latching step are combined in the transmission-gate pulsed latch (TGPL) [13], an example of such an implementation. When the master stage in TGFF is removed and the input data is sent to the output within a tiny pulse period induced by the clock edge, the DQ latency is reduced. Due to the circuit overhead needed to create the brief pulse, TGPL may use a significant amount of power despite its quick working. Problematic operation, especially in the NTV zone, may also result from the pulse width's unpredictability due to process factors. Though there have been significant improvements in pulse generation using novel circuit techniques, total power consumption is still greater than with TGFF when pulsed processes need internally delayed local clocks [14], [15].The employment of the sense-amplifier-based flip-flop (SAFF) method is another approach to increasing the speed of timing components [17]. Fast sampling and input data capture at the triggering clock edge are achieved by the flip-flop via the use of a symmetric latch and a differential precharged circuit in the first stage, respectively, allowing for high-speed operation. Altering the latching stage's architecture may increase power and speed even more, but it can also lead to undesirable signal fighting, which compromises latency

and power consumption [18]. Additionally, these flip-flops are vulnerable to increasing variability in the NTV area since they use a weak shorting mechanism to guarantee static functioning. Despite the fact that the issue may be resolved by monitoring the arrival of precharged nodes, there are significant power and latency overheads. This work introduces conditional bridging flip-flops (CBFFs), which are based on sensing amplifiers and may improve speed while lowering power consumption.

Fig:1. A) TGPL [13], (b) STPL [14], and



(c) DCPL [15] are pulsed latch-based FFs.

Problems with the previously mentioned shorting device are eliminated by the suggested conditional bridging method, which does not incur any power or speed overheads. A single-ended version (CBFF-S) of the flip-flop is suggested for decreasing power consumption, while a differential version (CBFF-D) is suggested for lowering latency. In addition to being fast, low-power, and contention-free, CBFFs can reliably operate in the NTV zone.

2. METHODOLOGY

2.1. SENSE-AMPLIFIER-BASED FLIP-FLOP

A. CONDITIONAL BRIDGING

A conditional bridging approach is suggested as a more power-efficient way to fix problems with the reducing device (M4) in traditional SAFFs. Motivated by the idea that the shorting device should only be activated when D changes after being collected by Q, the goal is to eradicate any relevant redundant transitions. In other situations, it is more prudent to disable the device in order to avoid the drawbacks of using an ineffective device and to avoid the unnecessary discharge of an internal node (X or Y) on the opposite branch. Figure shows the SA stage with a conditional bridging circuit, where the shorting device is driven by the circuit's output (CBG). The suggested conditional bridge circuit monitors the values of D, DB, SB, & RB to switch on M4 when CK=1 only when D changes & becomes

different from Q. Because SB & RB are pre-charged high when CK is low, activating M13, M17, and maybe one of M12 & M16, keeping CBG low is independent of the D value. Depending on the value of D, SB or RB discharge at the rising edge of the clock. Assuming SB is discharged, keeping CBG low by M16 – M17 is possible with D=RB=1. As soon as D goes low, CBG rises high via M14 and M15, enabling the activation of M4 to supply a DC route to the ground and guaranteeing static functioning.

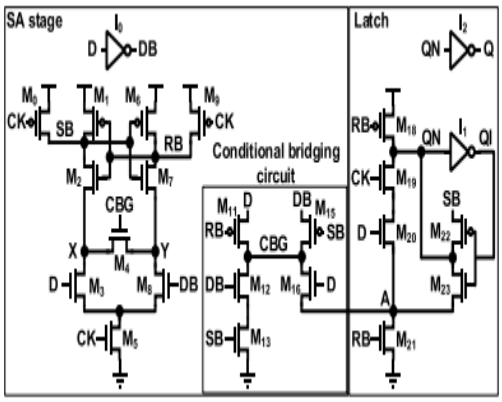


Fig:2. A flip-flop that just has one side open is another option.

B. STRUCTURE AND OPERATION

Two variants of the conditional-bridging flip-flop (CBFF) are suggested, both of which use the conditional bridging mechanism that was previously discussed. A sensing amplifier stage (M0-M9 and I0), a conditional bridging circuit (M11-M16) and a single-ended latch stage (M18- M23, I1, & I2) make up the single-ended version (CBFF-S), as shown in Figure 5. A reduction in the overall number of transistors in the flip-flop is achieved by modifying the conditional bridging circuit. More specifically, D drives M11's sources and DB's sources directly, whereas M15's sources are driven via DB. In Figure 5, the latch merges M21 and M17, which were controlled by RB in Figure 4, are shown. The glitch- & contention-free single-ended latch, powered by the SA stage without inversion (as indicated on the right portion of Fig.), allows the latching stage to be optimised for power consumption and device count. M18 uses just RB to pull-up QN following the rising clock edge, whereas M19–M21 uses only RB to pull-down QN. The purpose of inserting M20, which is driven by D, is to remove QN glitches caused by the precharged high value of RB at the beginning of the clock high frequency. In order to draw down QN without contention, SB is employed to drive the source of M22. Node A is likewise linked to the source of M23 so that QN may be pulled up without conflict. The lack of a pulsed operation distinguishes the latching stage of CBFF-S shown in Fig. from that of conventional pulsed latches [13], [14], [15].

Choose CBFF-S if you care about operational reliability, latency, and power usage. One way to avoid unnecessary CBG

transitions is to control when the conditional bridging logic engages the shorting device (M4). At low switching activity, the conditional bridging circuit will minimise power consumption because it transitions when D changes after Q grabs D during CK=1. The circuit allows for miniaturisation by reducing power consumption and preventing shorting. To save power, CBFF-S only releases the opposing precharge node (X or Y) if D changes, as D seldom changes under low input switching activity. Regular SAFFs charge and discharge them on a clock cycle, as previously mentioned. The smallest possible shorting device might potentially decrease latency and draw out timing-critical impulses like SB and RB quicker due to its smaller parasitic capacitance. Disabling the shorting device allows for faster input sampling by eliminating SB-RB signal interference. Through direct control of the latching process, RB eliminates signal inversion and contention, hence decreasing clock-to-output (CQ) time. Pulling down pre charged nodes reliably at low supply voltages is made possible by reducing congestion in the SA stage. CBFF-S's contention-free latching stage & conditional-bridging SA stage ensure input data is securely gathered while the system operates steadily in the highly volatile NTV zone. Presented here is the differential suggested flip-flop, often known as CBFF-D. Figure 13 shows two transistors, M13 and M30, that may be combined in the conditional bridging circuit without the need to add a third transistor because of the symmetric differential structure. When we add a few transistors after latching and remove the output inverter (I2 in Fig.), we can tell SB and RB to drive difference outputs Q , QB. Putting CK-powered M24 in parallel to pull-up keepers transistors M22 and M25 speeds up output pull-down by stopping them from struggling. While a setup comparable to the single-ended variant (M22 powered by SB in Fig) performs well at normal supply voltages, the inclusion of a delayed transistor (M24) is necessitated due to reliability concerns highlighted by Monte-Carlo simulations in the worst corners. In terms of operation speed and power consumption, CBFF-D is identical to its single-ended predecessor. Despite having a slightly higher overall power consumption owing to the bigger load capacitance of CK utilised to operate the differential latch, CBFF-D greatly decreases power usage in low-activity switching scenarios with its conditional bridging function. Due to the SA the stage's outputs driving Q and QB different latches, CBFF-D can outperform CBFF-S in terms of speed.

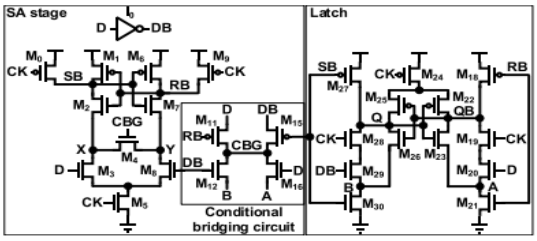


Fig:3. The suggested flip-flop in its differential form.

3. RESULTS

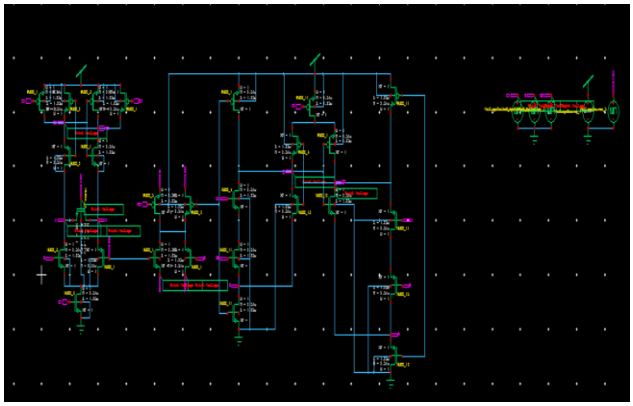


Fig:4. Schematic of Single-ended version flip-flop

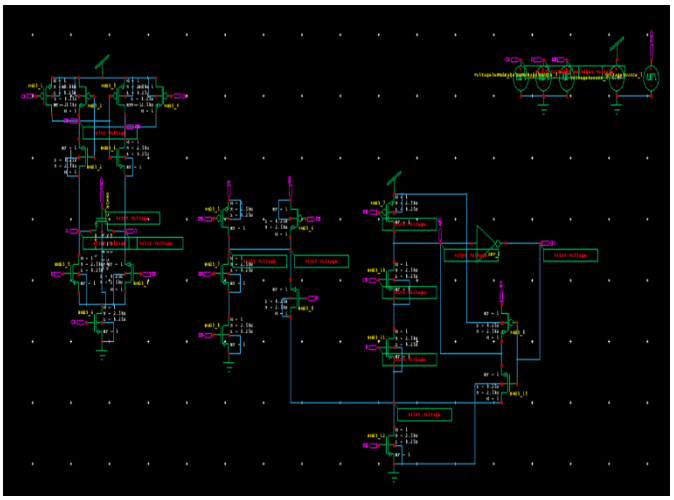


Fig:5. schematic of Differential version flip-flop.

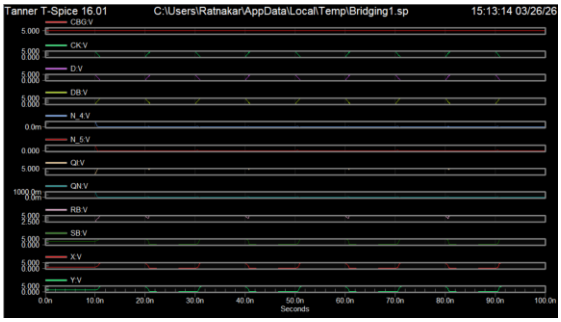


Fig 6: bridging output waveform.

Averaging 8.1984W, the system's power usage trends were all over the place. During this time, power usage varied from 0.00000W at the lowest to 1.7371W at the highest. A setup time of 0.03 seconds was reported for the system to stabilise, which is in close agreement to the DC operating point. The system's settling into a steady state was indicated by a transitory phase lasting 0.39 seconds, according to further investigation.

4. CONCLUSION

The paper introduces sense amplifier-based flip-flops that are dependable, high-performance, and power-efficient. In order to avoid unnecessary transitions and maintain static operation, the proposed conditional bridging adaptively activates the shorting device. Making the shorting device as tiny as feasible may therefore lower the effective capacitance parasite along the timing-critical signal paths. Power consumption and time are both drastically reduced when the locking step is driven directly without glitches

or conflicts. To optimise power consumption and space, the single-ended variation of the recommended flip-flop uses a revised latching step. Optimal performance and differential operation are achieved by introducing the differential version, which incorporates a differential latching step. The proposed flip-flops are capable of stable operation all the way down to the NTV region, and they also offer superior power and latency performance. A performance analysis employing 18-nm CMOS technology revealed that the proposed flip-flops performed admirably, indicating that they might be valuable in low-power, high-speed digital applications. For aggressive voltage scaling to the region surrounding the threshold voltage without considerably lowering performance, a new constrained bandgap filter (CBFF) has been presented. This project introduces a pulse trigger FF design that is perfect for low power applications using a boost body driven approach. Last but not least, we provide the concept of a multibit flip-flop combined with a conditional boosting flip-flop, which effectively improves power area and latency.

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